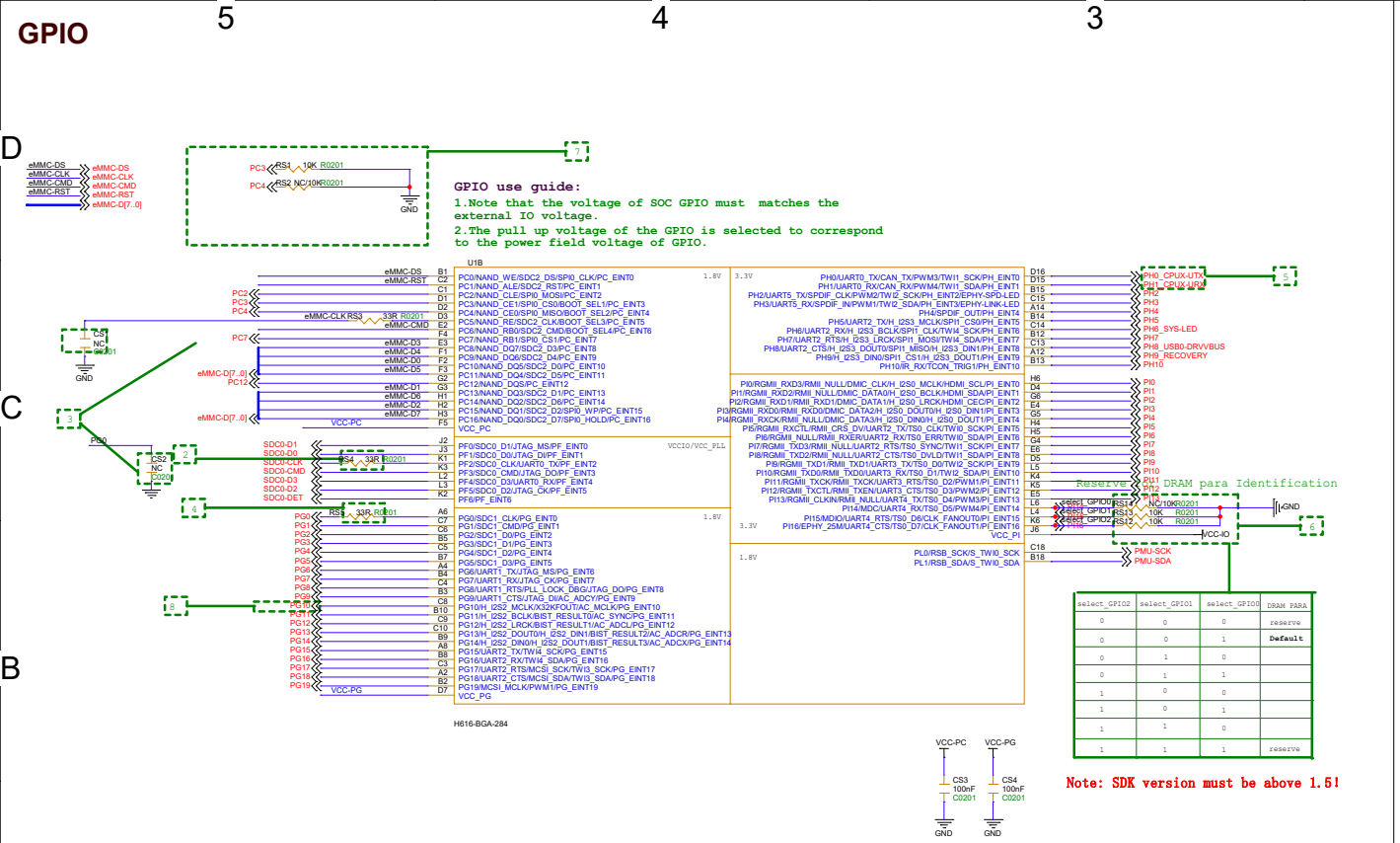
REVISION HISTORY

Revision	Description	Date
Ver 1.0	Initial Version	2023-11-27

SiPEED 矽速科技

Page Name: Revision History

Size	Project Name - Rev	Designer: ‹Designer›
A3	LM3H	Checker: ‹Checker›
Date: Monday, November 27, 2023		Sheet 1 of 1



SOC and peripheral circuit considerations-1

1. RS3 is the termination resistor at the source end of EMMC-CLK, which cannot be deleted.

2. RS4 is the termination resistor of SDCO-CLK source end, which cannot be deleted.

3. CS1 and CS2 are reserved for EMI suppression and need to be placed close to the Device.

4. RS5 is the termination resistor of SDIO-CLK source end, which cannot be deleted.

5. The default function of PH0 and PH1 is the UART print port, which is used for system software debugging and cannot be changed.

6. The DRAM para version identification reserved circuit cannot be deleted. For the purpose of software normalization management, the same firmware is compatible with multiple DRAM templates and DRAM materials. The way to read the hardware GPIO level in the boot phase, the software automatically calls the corresponding DRAM para. Pay special attention to the one-to-one correspondence between BOM and DRAM para.

7. boot sel: BROM will read the state of BOOT_Select, choose the external storage medium to boot, and speed up the boot time.
H616 has 4 boot sel pins multiplexed with the PC port, the configuration relationship is as follows:

bit[10]	bit[11]	bit[12]	bit[13]	Media	
1	1	1	1	MLC/SLC NAND	
0	1	1	1	eMMC USER	Default
1	0	1	1	eMMC BOOT	
1	1	0	1	SPI NOR	
1	1	1	0	SPI NAND	

The multiplexing relationship between 4 boot sel and PC port is as follows:
Bit[10]->PC3
Bit[11]->PC4
Bit[12]->PC5
Bit[13]->PC6

8. 32K clock fanout, output low frequency clock, can be used by external wifi module, needs to surrounded by GND.

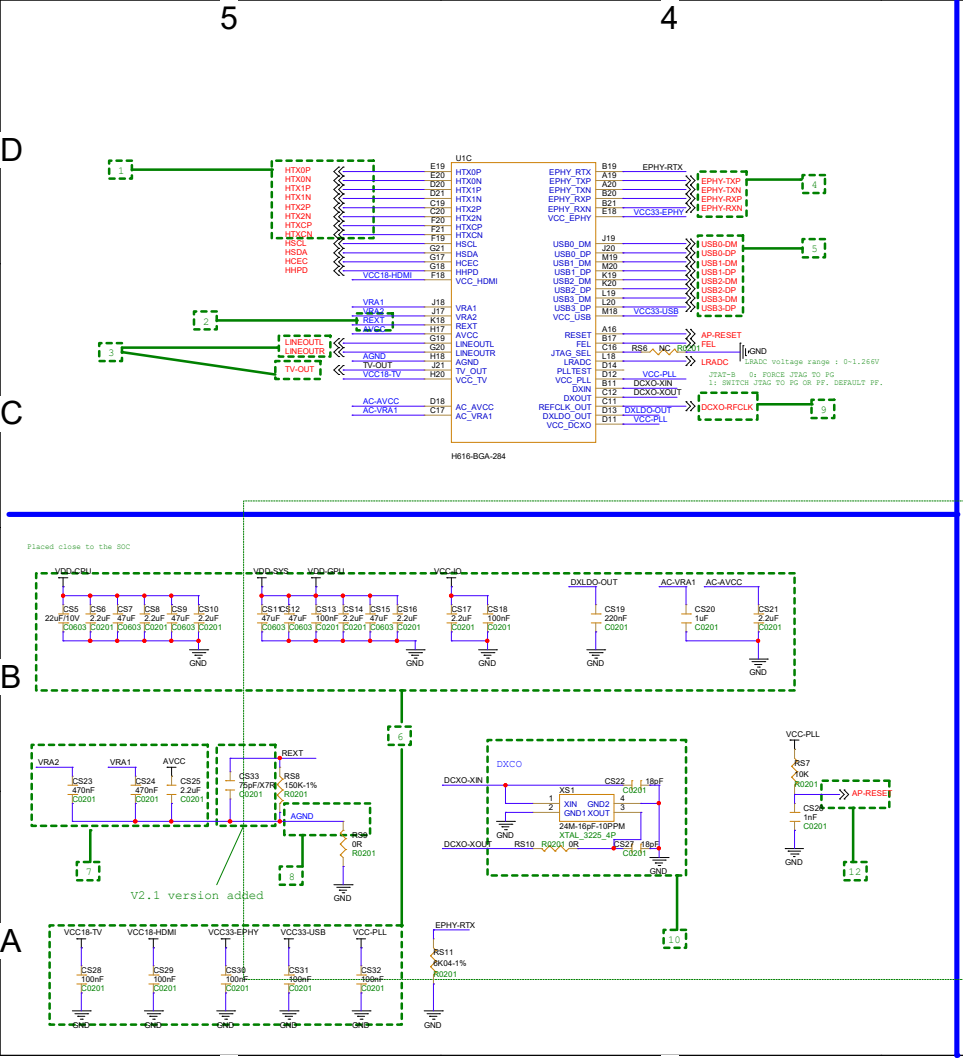
GPIO power domain list:

GROUP	Power Field	Voltage(V)
PC	VCC-PC	1.8/3.3
PF	VCC-PLL/VCC-IO	1.8/3.3
PG	VCC-PG	1.8/3.3
PH	VCC-IO	3.3
PI	VCC-PI	1.8/3.3
PL	VCC-PLL	1.8

Note: 1. When GPIO is not used, it can be directly floated, and the software is set to Disable.
2. After changing the default voltage of the multi-voltage IO power supply, the corresponding configuration changes must be confirmed on the software.

SiPEED 矽速科技

Page Name	SOC1		
Size: Custom	Project Name - Rev: LM3H	Designer:	
		Checker:	
Date: Monday, November 27, 2023		Sheet 2 of 1	



SOC and peripheral circuit considerations-2

1. The HDMI differential signal controls the differential impedance of 100ohm.

2. REXT is a sensitive signal, and the layout path is kept to the shortest.

3. Lineout, TVOUT individually ground; TVOUT trace control impedance 37.5ohm.

4. ePHY differential signal control differential impedance 100ohm.

5. USB differential signal control differential impedance 90ohm.

6. The decoupling capacitance of each module has been optimized by PI and cannot be modified.

7. The bypass capacitor of CODEC cannot be modified. These parameters will affect the internal power-on sequence.

8. The AGND trace should be as wide as possible, at least 12mil or more, and the copper skin should be widened after the BGA is released; the number of R99 GND vias should be guaranteed at least two.

9. 24Mfanout clock, can be used for wifi module, and the wiring needs to be isolated with ground.

10. The crystal matching capacitor is the reference value, the actual capacitance value can be modified according to the test; in addition, the series resistance needs to be reserved to facilitate debugging the oscillation amplitude.

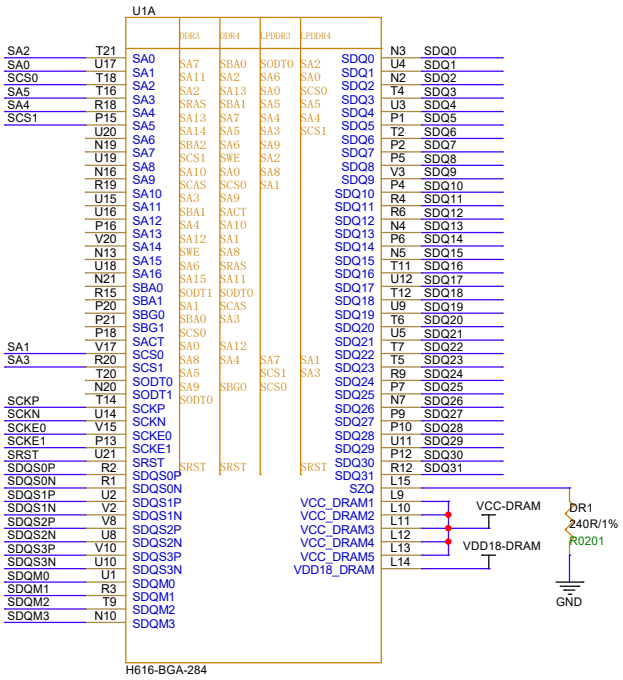
11. The voltage feedback test point should be placed near the projection area of the back of the power pin.

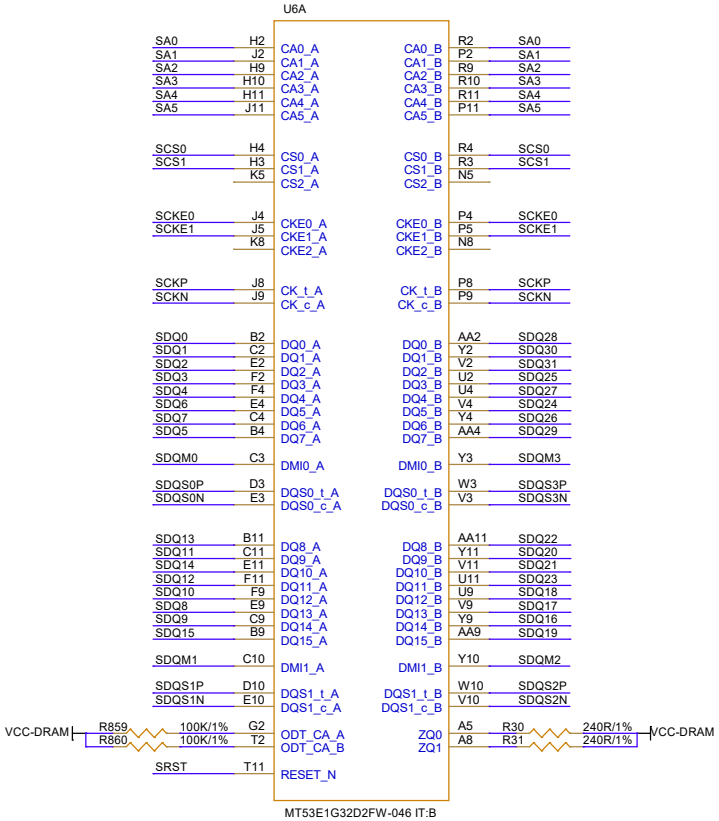
12. The system reset signal AP-reset is far away from the board edge and interference signals.

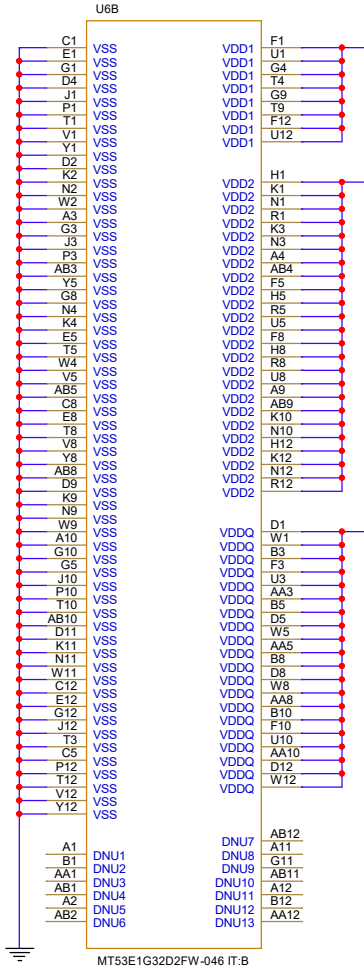
SiPEED 矽速科技

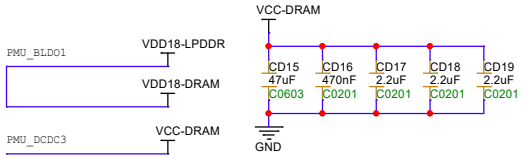
Page Name	SOC2		
Size: Custom	Project Name - Rev: LM3H	Designer:	
		Checker:	
Date: Monday, November 27, 2023		Sheet 3 of 1	

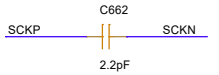
LPDDR4

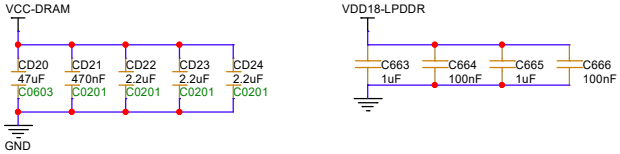


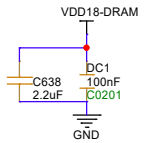


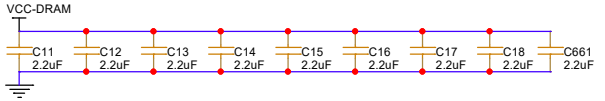


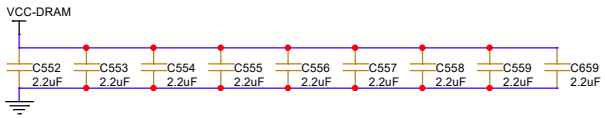


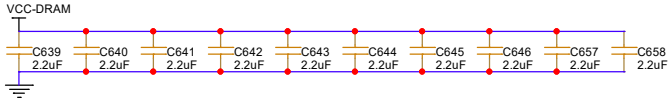


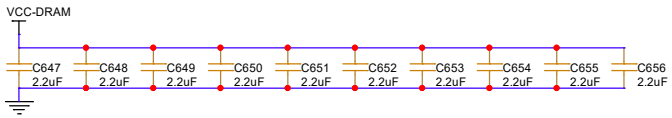










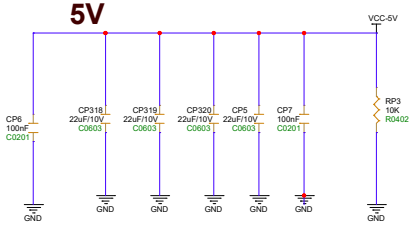


SiPEED 矽速科技

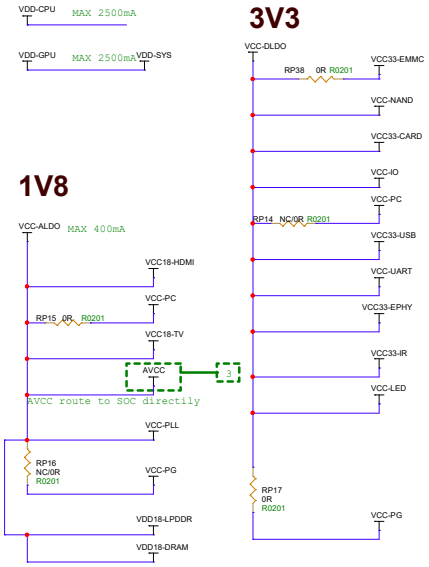
Page Name	LPDDR4
Size	A3
Project Name - Rev	LM3H
Designer	‹Designer›
Checker	‹Checker›
Date	Monday, November 27, 2023
Sheet	4 of 1

DCIN

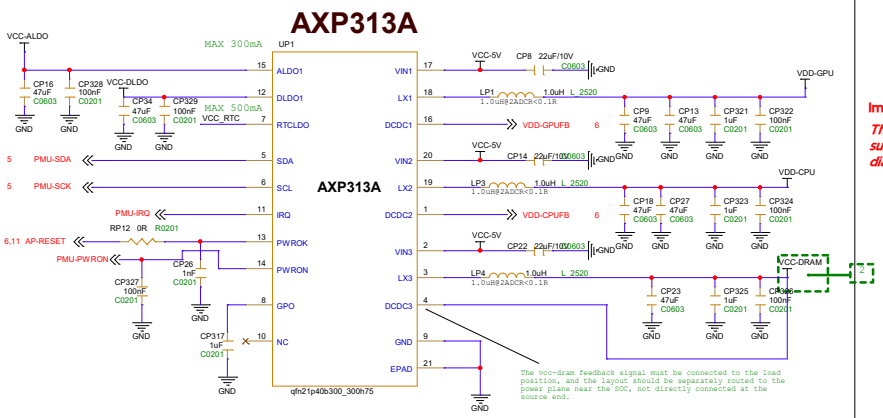
5V



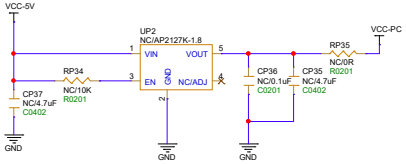
3V3



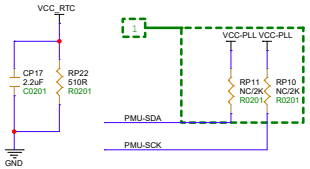
AXP313A



Option1:



Reserve for EMMC which 1.8V current greater than 300mA.



Power design considerations

1. AXP313A is controlled by the I2C signal of the PL port, and the external needs to be reserved for pull-up to VCC-PLL.

2.VCC-DRAM can support DDR3, DDR4, LPDDR3, LPDDR4 different DRAM power supply, different DRAM types through software
The identification is automatically matched to the appropriate supply voltage.

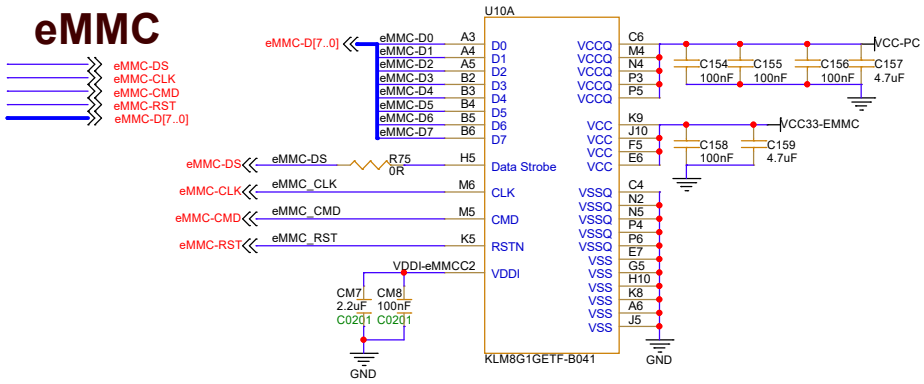
3. AVCC supplies power for analog modules such as Audio codec, T-senor, etc. The accuracy must be +/ - 1%, and the minimum power supply voltage cannot be lower than 1.78V.
Otherwise, it will affect Audio performance and sensor accuracy.

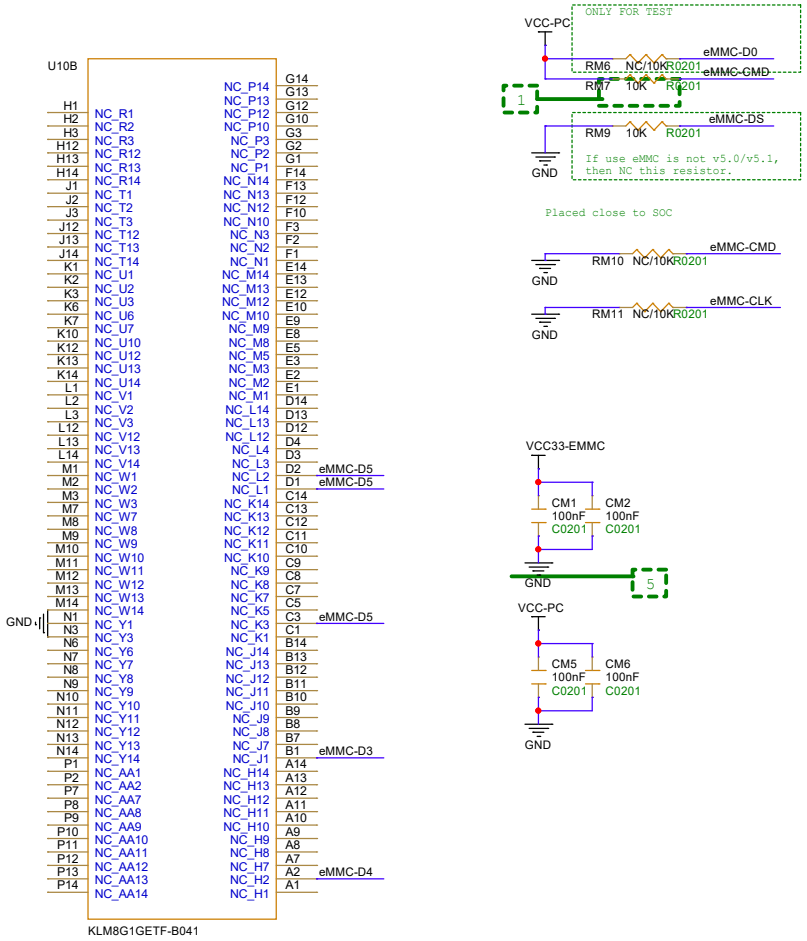
Important:

The stability of the power supply directly affects the stability of the system. Please be sure to refer to the relevant guide in the "Hardware Design Guide" for the schematic diagram and PCB design!

SiPEED 矽速科技

Page Name	POWER		
Size: Custom	Project Name - Rev: LM3H	Designer: <Designer>	
		Checker: <Checker>	
Date: Monday, November 27, 2023		Sheet 5 of 1	





Flash design considerations

1. CMD needs to be pulled up to VCC-PC.

2. The reserved pins, such as eMMCNC / RFU, are left unconnected. Do not connect these signals with power, ground, or other eMMC signals for easy fanout.

3. If you use Sandisk or Toshiba's nandflash, you need to pull up VPS0 and VPS1, and the other is left floating by default.

4. Some nand have 1.8V power supply, these two pins need to be connected to VCC-PC.

5. The EMMC IO power supply voltage matches the power domain voltage of the SOC GPIO.

Important:

For the PCB design of the Flash module, please refer to the layout guide in the Hardware Design Guide,
The guide has detailed impedance, timing and crosstalk requirements;
Note that when EMMC and NAND are dual-layout, a daisy-chain topology is used, and EMMC is used as a routing terminal.

SiPEED 矽速科技

Page Name	eMMC
Size	A3
Project Name - Rev	LM3H
Designer	<Designer>
Checker	<Checker>
Date	Monday, November 27, 2023
Sheet	6 of 1

J2

TV-OUT	2	TV-OUT			
GND	4	GND			
LRADC	6	LRADC			
LINEOUTR	8	LINE_OUT_R			
LINEOUTL	10	LINE_OUT_L			
GND	12	GND			
USB2-DP	14	USB2-DP			
USB2-DM	16	USB2-DM			
GND	18	GND			
USB0-DP	20	USB0-DP			
USB0-DM	22	USB0-DM			
GND	24	GND			
USB3-DP	26	USB3-DP			
USB3-DM	28	USB3-DM			
GND	30	GND			
USB1-DP	32	USB1-DP			
USB1-DM	34	USB1-DM			
GND	36	GND			
PI2	38	PI2/RGMII_RXD1/RMII_RXD1/DMIC_DATA1/H_I2S0_LRCK/HDMI_CEC/PI_EINT2			
PI4	40	PI4/RGMII_RXCK/RMII_NULL/DMIC_DATA3/H_I2S0_DIN0/H_I2S0_DOUT1/PI_EINT4			
PI8	42	PI8/RGMII_TXD2/RMII_NULL/UART2_CTS/TS0_DVLD/TWI1_SDA/PI_EINT8			
PI13	44	PI13/RGMII_CLKIN/RMII_NULL/UART4_TX/TS0_D4/PWM3/PI_EINT13			
PI9	46	PI9/RGMII_TXD1/RMII_TXD1/UART3_TX/TS0_D0/TWI2_SCK/PI_EINT9			
PI1	48	PI1/RGMII_RXD2/RMII_NULL/DMIC_DATA0/H_I2S0_BCLK/HDMI_SDA/PI_EINT1			
PI15	50	PI15/MDIO/UART4_RTS/TS0_D6/CLK_FANOUT0/PI_EINT15			
PI10	52	PI10/RGMII_TXD0/RMII_TXD0/UART3_RX/TS0_D1/TWI2_SDA/PI_EINT10			
PI11	54	PI11/RGMII_TXCK/RMII_TXCK/UART3_RTS/TS0_D2/PWM1/PI_EINT11			
PI14	56	PI14/MDC/UART4_RX/TS0_D5/PWM4/PI_EINT14			
			GND	1	GND
			GND	3	
			GND	5	
			GND	7	
			GND	9	
			GND	11	
			GND	13	
			5V-VIN	15	VCC-5V
			5V-VIN	17	
			5V-VIN	19	
			5V-VIN	21	
			5V-VIN	23	
			5V-VIN	25	
			3V3-DLDO-OUT	27	VCC-DLDO
			1V8-ALDO-OUT	29	VCC-ALDO
			PMU-PWRON	31	PMU-PWRON
			PMU-IRQ	33	PMU-IRQ
			PL0/RSB_SCK/S_TWI0_SCK	35	PMU-SCK 5
			PL1/RSB_SDA/S_TWI0_SDA	37	PMU-SDA 5
			NC	39	
			NC	41	
			NC	43	
			NC	45	
			NC	47	
			NC	49	
			NC	51	
			NC	53	
			NC	55	
			PH3/UART5_RX/SPDIF_IN/PWM1/TWI2_SDA/PH_EINT3/EPHY-LINK-LED	57	PH3
			PG12/H_I2S2_LRCK/BIST_RESULT1/AC_ADCL/PG_EINT12		PG12
PI16	68	PI16/EPHY_25M/UART4_CTS/TS0_D7/CLK_FANOUT1/PI_EINT16			
PI12	70	PI12/RGMII_TXCTL/RMII_TXEN/UART3_CTS/TS0_D3/PWM2/PI_EINT12			
PI5	72	PI5/RGMII_RXCTL/RMII_CRS_DV/UART2_TX/TS0_CLK/TWI0_SCK/PI_EINT5			
PI6	74	PI6/RGMII_NULL/RMII_RXER/UART2_RX/TS0_ERR/TWI0_SDA/PI_EINT6			
			PF5/SDC0_D2/JTAG_CK/PF_EINT5	67	
			PF4/SDC0_D3/UART0_RX/PF_EINT4	69	SDC0-D2
			PF6/PF_EINT6	71	SDC0-D3
			PF2/SDC0_CLK/UART0_TX/PF_EINT2	73	SDC0-DET
			PF3/SDC0_CMD/JTAG_DO/PF_EINT3	75	SDC0-CLK
					SDC0-CMD

CON_NGFF_M_KEY_LM3H_P1

M1

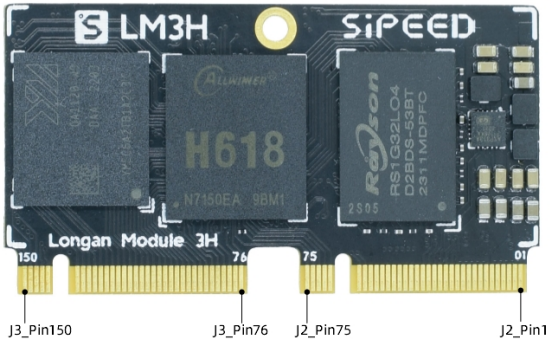
GND

Mounting_Hole

J3

PI0	77	PI0/RGMII_RXD3/RMII_NULL/DMIC_CLK/H_I2S0_MCLK/HDMI_SCL/PI_EINT0			
PI7	79	PI7/RGMII_TXD3/RMII_NULL/UART2_RTS/TS0_SYNC/TWI1_SCK/PI_EINT7			
PC7	81	PC7/NAND_RB1/SPI0_CS1/PC_EINT7			
PI3	83	PI3/RGMII_RXD0/RMII_RXD0/DMIC_DATA2/H_I2S0_DOUT0/H_I2S0_DIN1/PI_EINT3			
HCEC	85	HCEC			
HHPD	87	HHPD			
GND	89	GND			
HTX2P	91	HTX2P			
HTX2N	93	HTX2N			
GND	95	GND			
HTX1P	97	HTX1P			
HTX1N	99	HTX1N			
GND	101	GND			
HTXCP	103	HTXCP			
HTXCN	105	HTXCN			
GND	107	GND			
HTX0P	109	HTX0P			
HTX0N	111	HTX0N			
GND	113	GND			
HSDA	115	HSDA			
HSCL	117	HSCL			
GND	119	GND			
EPHY-RXN	121	EPHY-RXN			
EPHY-RXP	123	EPHY-RXP			
GND	125	GND			
EPHY-TXN	127	EPHY-TXN			
EPHY-TXP	129	EPHY-TXP			
GND	131	GND			
			PF0/SDC0_D1/JTAG_MS/PF_EINT0	76	
			PF1/SDC0_D0/JTAG_DI/PF_EINT1	78	SDC0-D1
			PC12/NAND_DQS/PC_EINT12	80	SDC0-D0
			PC3/NAND_CE1/SPI0_CS0/BOOT_SEL1/PC_EINT3	82	PC12
			PC4/NAND_CE0/SPI0_MISO/BOOT_SEL2/PC_EINT4	84	PC3
			PC2/NAND_CLE/SPI0_MOSI/PC_EINT2	86	PC4
			PG19/MCSI_MCLK/PWM1/PG_EINT19	88	PC2
			PG18/UART2_CTS/MCSI_SDA/TWI3_SDA/PG_EINT18	90	PG19
			PG17/UART2_RTS/MCSI_SCK/TWI3_SCK/PG_EINT17	92	PG18
			PG9/UART1_CTS/JTAG_DI/AC_ADCY/PG_EINT9	94	PG17
			PG7/UART1_RX/JTAG_CK/PG_EINT7	96	PG9
			PG6/UART1_TX/JTAG_MS/PG_EINT6	98	PG7
			PG8/UART1_RTS/PLL_LOCK_DBG/JTAG_DO/PG_EINT8	100	PG6
			PG3/SDC1_D1/PG_EINT3	102	PG8
			PG0/SDC1_CLK/PG_EINT0	104	PG3
			PG4/SDC1_D2/PG_EINT4	106	PG0
			PG2/SDC1_D0/PG_EINT2	108	PG4
			PG5/SDC1_D3/PG_EINT5	110	PG2
			PG1/SDC1_CMD/PG_EINT1	112	PG5
			PG15/UART2_TX/TWI4_SCK/PG_EINT15	114	PG1
			PG16/UART2_RX/TWI4_SDA/PG_EINT16	116	PG15
			PG10/H_I2S2_MCLK/X32KFOUT/AC_MCLK/PG_EINT10	118	PG16
			PG14/H_I2S2_DIN0/H_I2S2_DOUT1/BIST_RESULT3/AC_ADCX/PG_EINT14	120	PG10
			PH9/H_I2S3_DIN0/SPI1_CS1/H_I2S3_DOUT1/PH_EINT9	122	PG14
			PH7/UART2_RTS/H_I2S3_LRCK/SPI1_MOSI/TWI4_SDA/PH_EINT7	124	PH9_RECOVERY
			PH8/UART2_CTS/H_I2S3_DOUT0/SPI1_MISO/H_I2S3_DIN1/PH_EINT8	126	PH7
			PH10/IR_RX/TCON_TRIG1/PH_EINT10	128	PH8_USB0-DRVVBUS
			PH4/SPDIF_OUT/PH_EINT4	130	PH10
			PH5/UART2_TX/H_I2S3_MCLK/SPI1_CS0/PH_EINT5	132	PH4
					PH5
PH1_CPUX-URX	143	PH1/UART0_RX/CAN_RX/PWM4/TWI1_SDA/PH_EINT1			
PH0_CPUX-UTX	145	PH0/UART0_TX/CAN_TX/PWM3/TWI1_SCK/PH_EINT0			
AP-RESET	147	AP-RESET			
FEL	149	FEL			
			PG13/H_I2S2_DOUT0/H_I2S2_DIN1/BIST_RESULT2/AC_ADCR/PG_EINT13	142	
			PG11/H_I2S2_BCLK/BIST_RESULT0/AC_SYNC/PG_EINT11	144	PG13
			PH6/UART2_RX/H_I2S3_BCLK/SPI1_CLK/TWI4_SCK/PH_EINT6	146	PG11
			PH2/UART5_TX/SPDIF_CLK/PWM2/TWI2_SCK/PH_EINT2/EPHY-SPD-LED	148	PH6_SYS-LED
			GND	150	PH2
					GND

CON_NGFF_M_KEY_LM3H_P2



SiPEED 矽速科技

Page Name	GoldenFinger		
Size B	Project Name – Rev LM3H	Designer: ‹Designer›	
		Checker: ‹Checker›	
Date:	Wednesday, November 29, 2023	Sheet 7 of 1	