

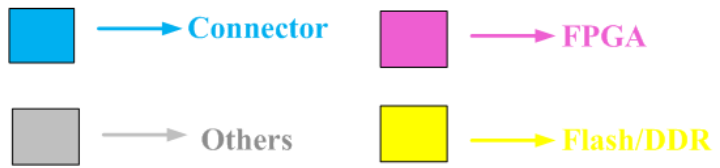
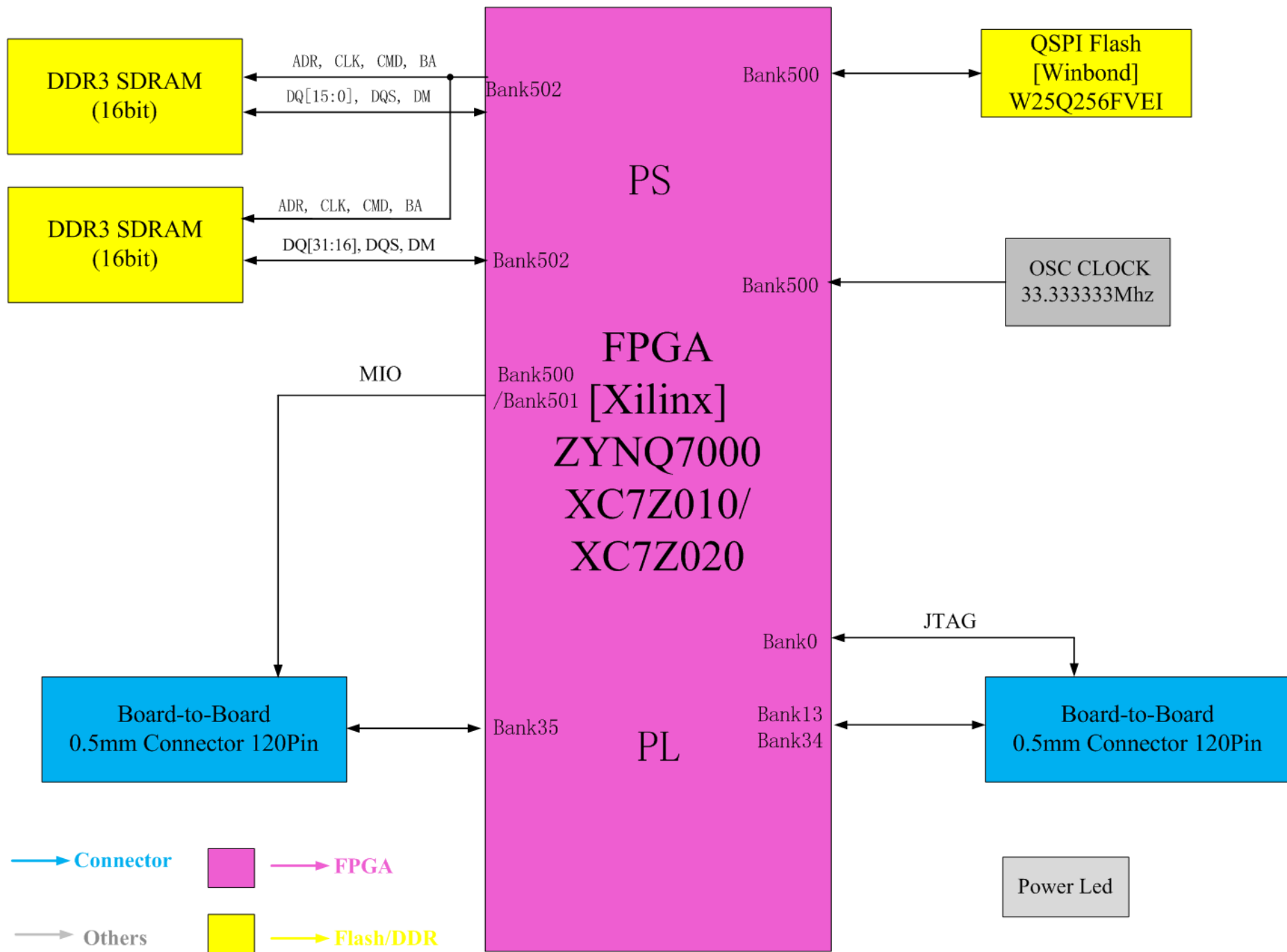
REV	Description	Date
V1.0	First Release	2019-6-21

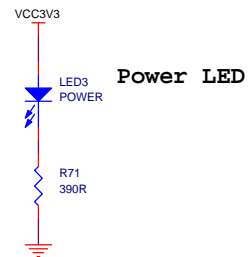
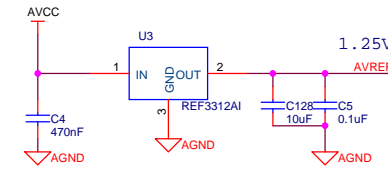
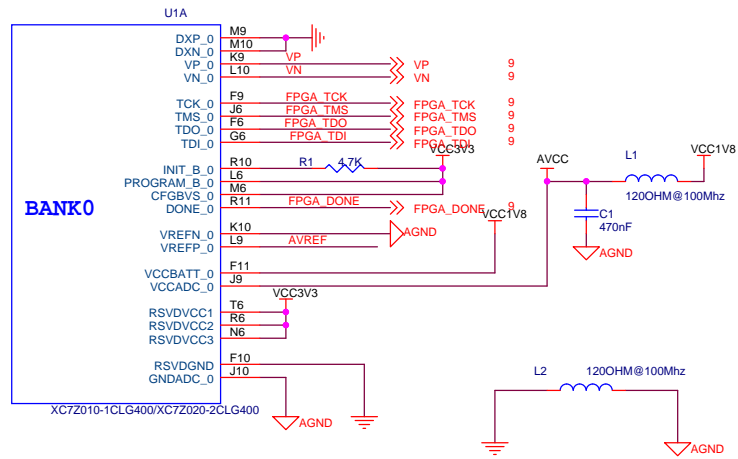
AC7Z010/AC7Z020 Schematics

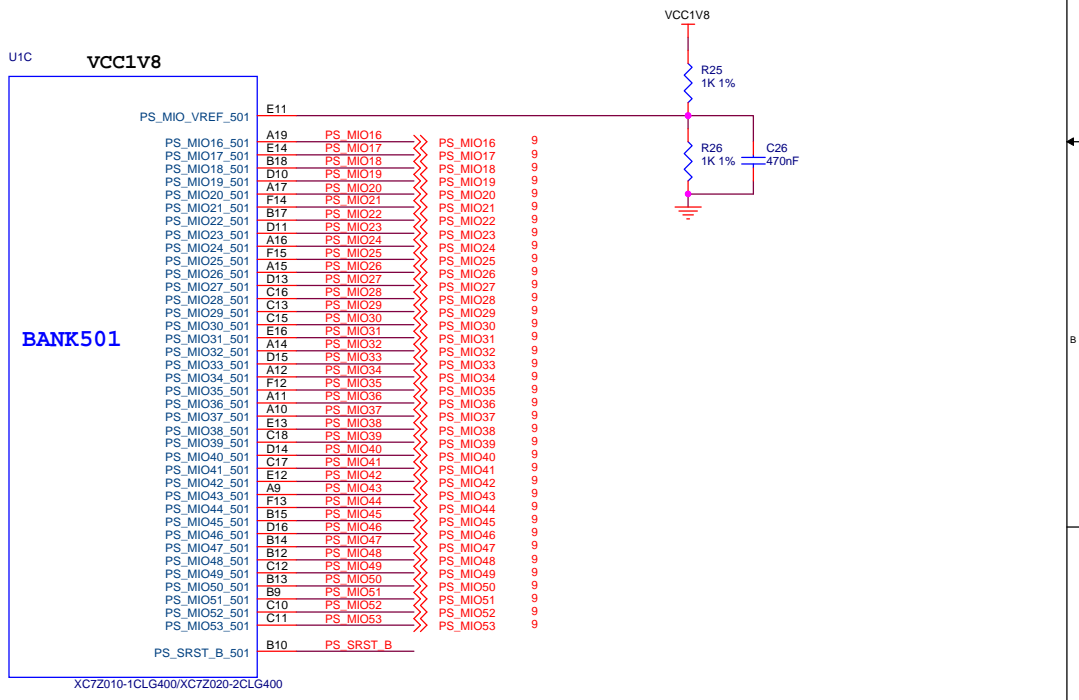
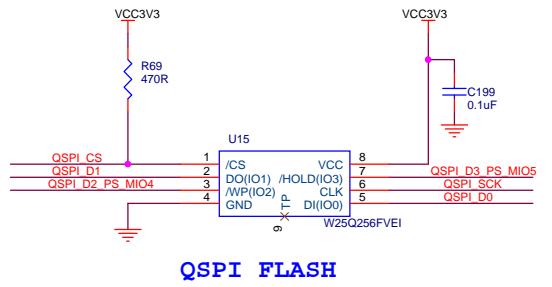
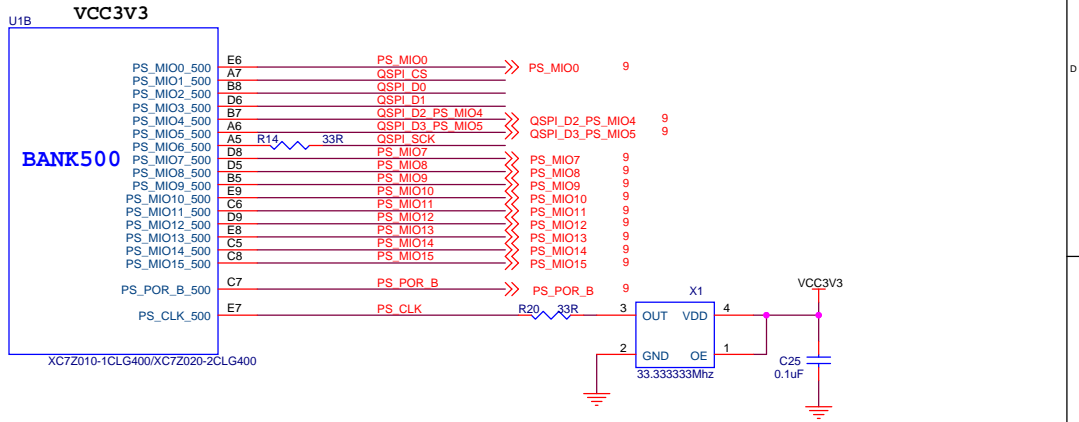
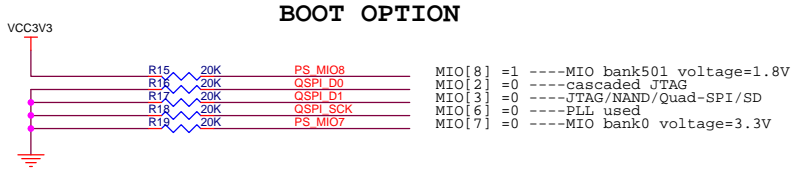
ZYNQ硬件平台

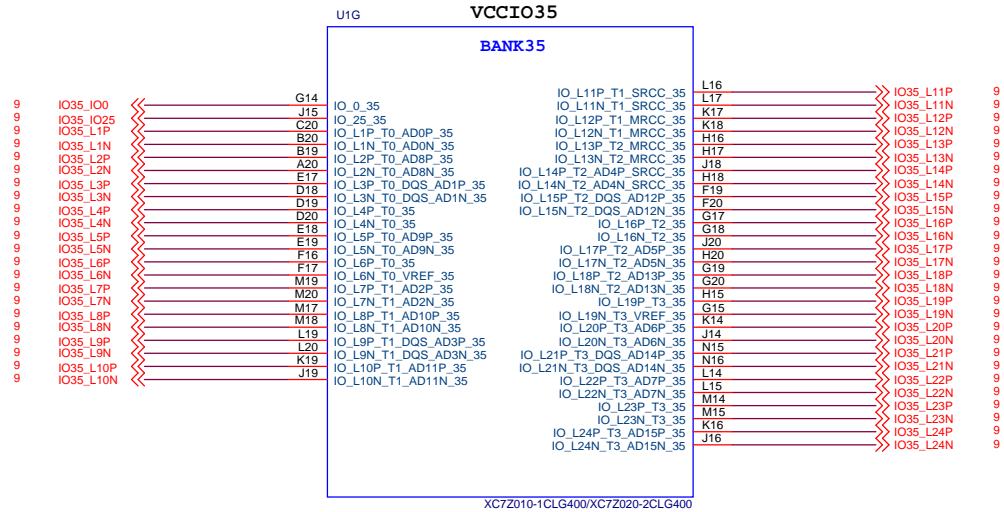
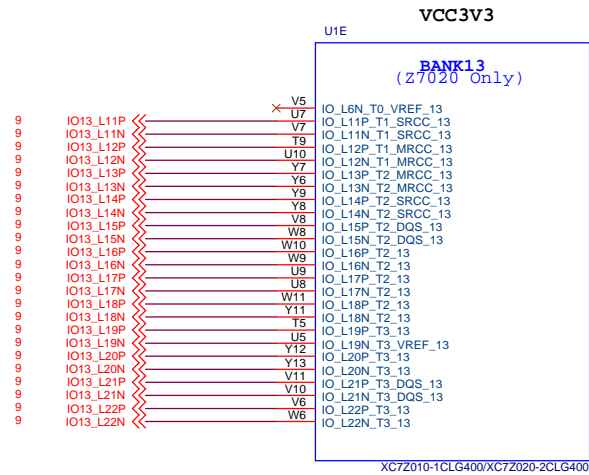
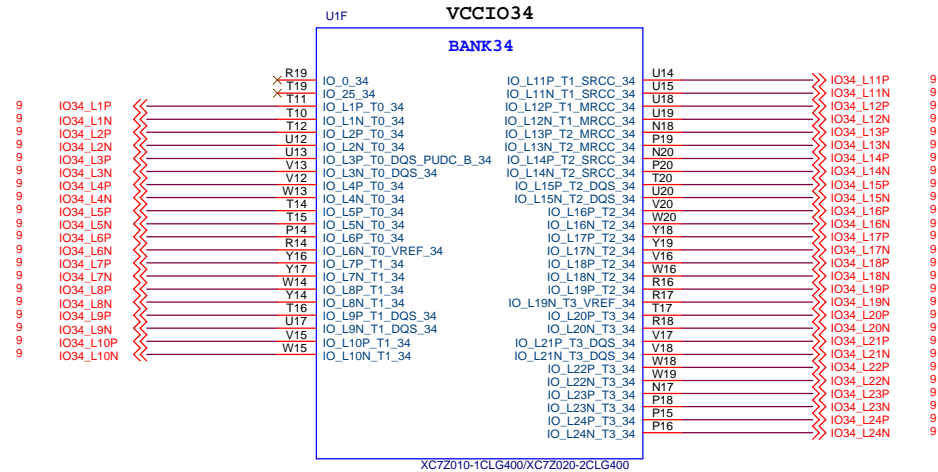
Page Number	Description
Page01	Cover Page
Page02	Block Diagram
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Page04	Zynq-7000 MIO Config
Page05	Zynq-7000 Bank13-34-35
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Page07	Zynq-7000 Power
Page08	DDR3
Page09	GPHY
Page10	USB OTG
Page11	UART, SD
Page12	EXTEND IO
Page13	POWER

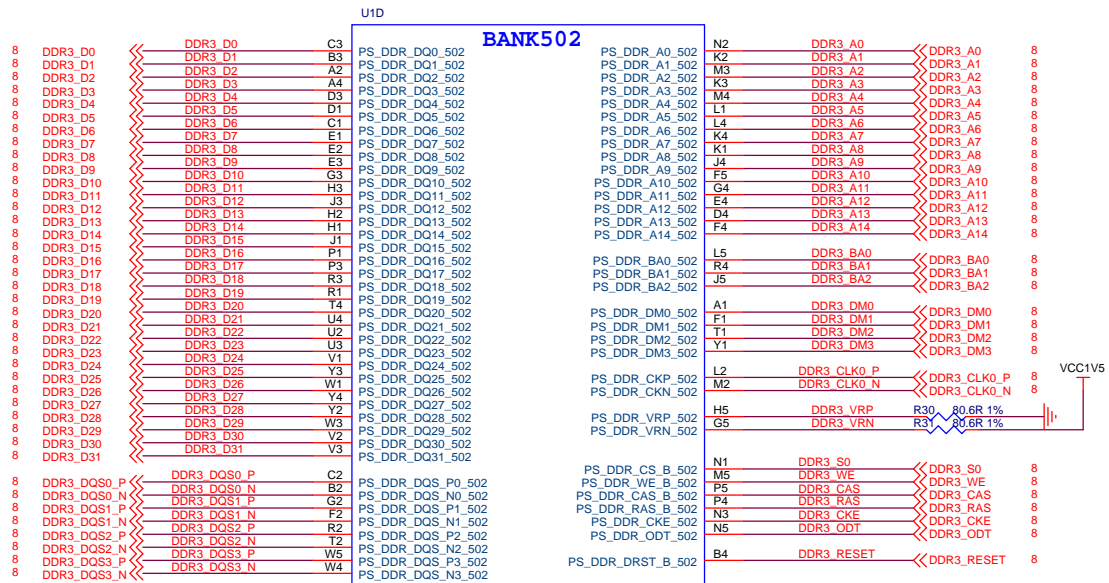
ALINX		
Title	Zynq-7000 Cover Page	
Size	Document Number	Rev
	AC7Z010/AC7Z020 核心板Schematics	1.0
Date:	Wednesday, August 21, 2019	Sheet 1 of 13



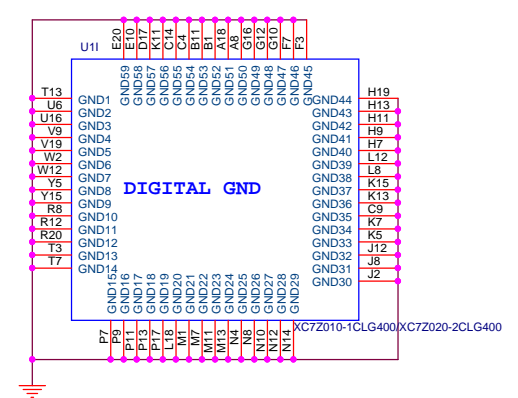
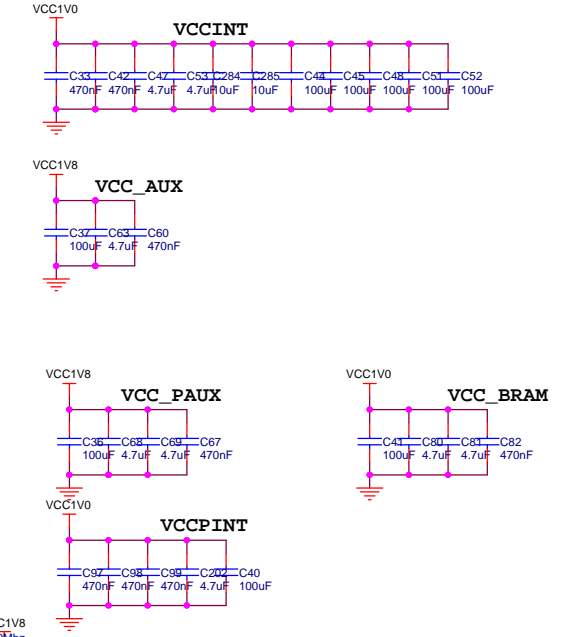
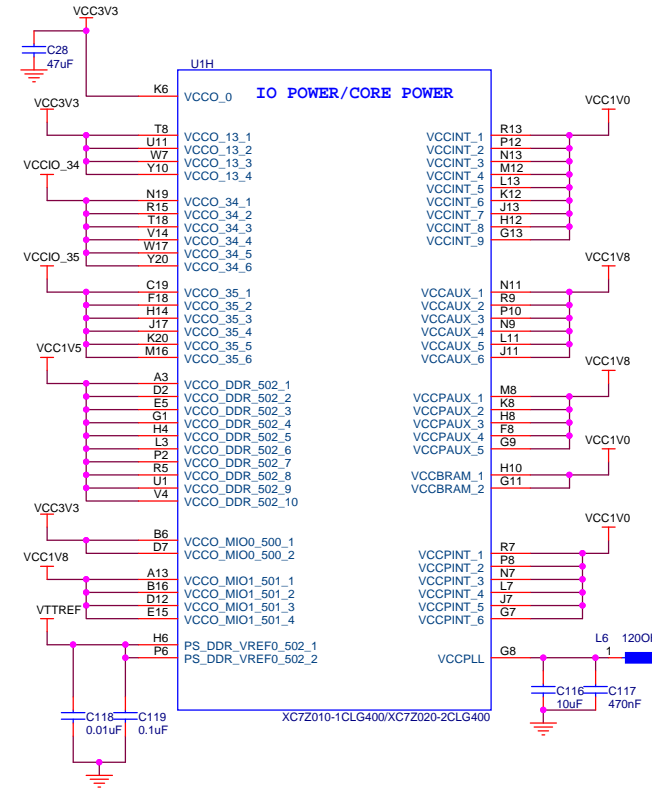
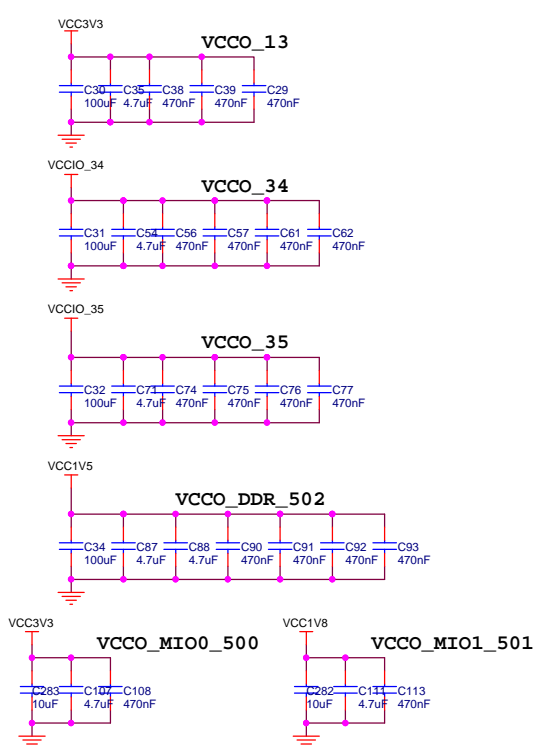


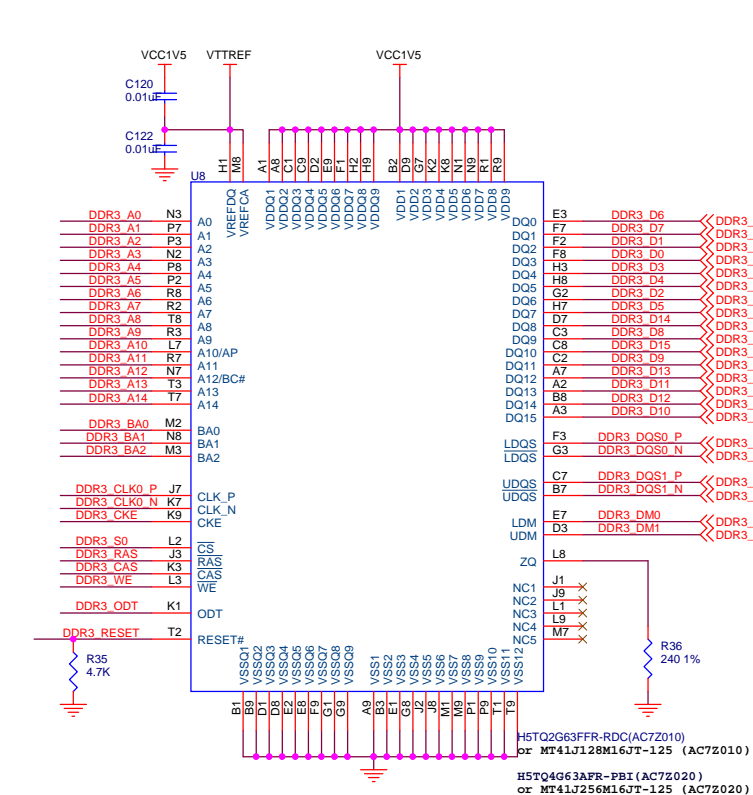
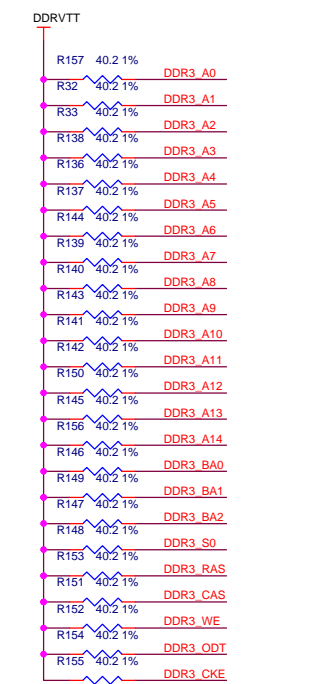
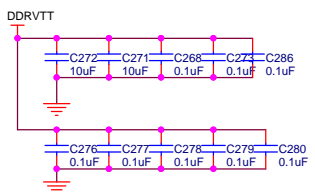




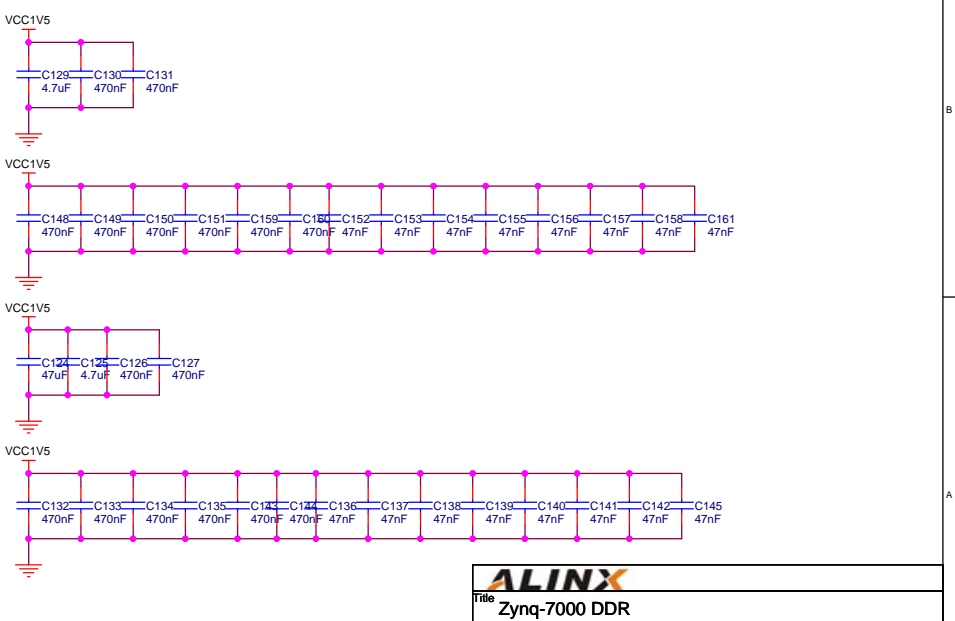
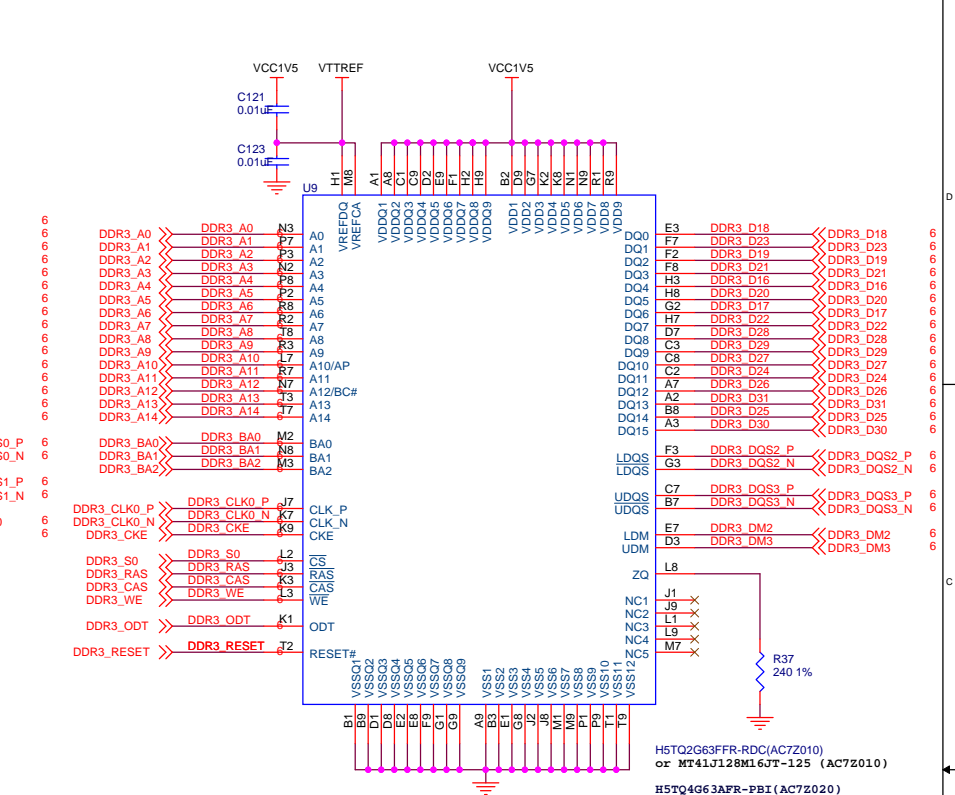
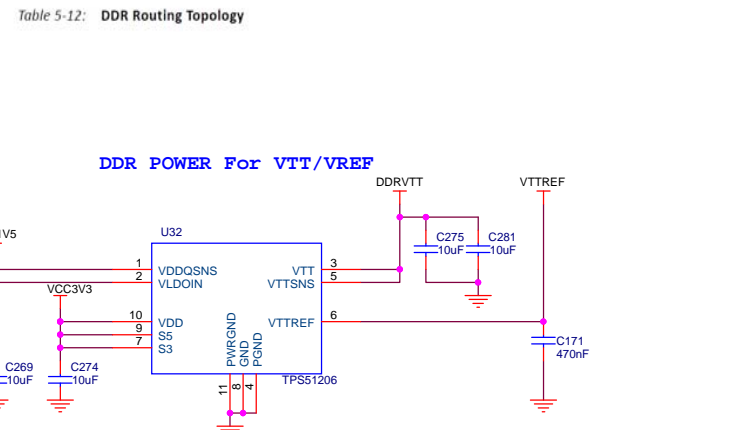
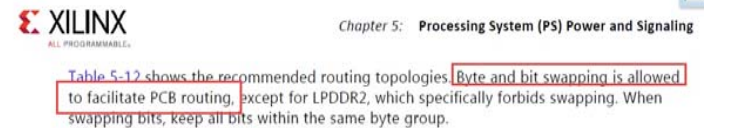


XC7Z010-1CLG400/XC7Z020-2CLG400

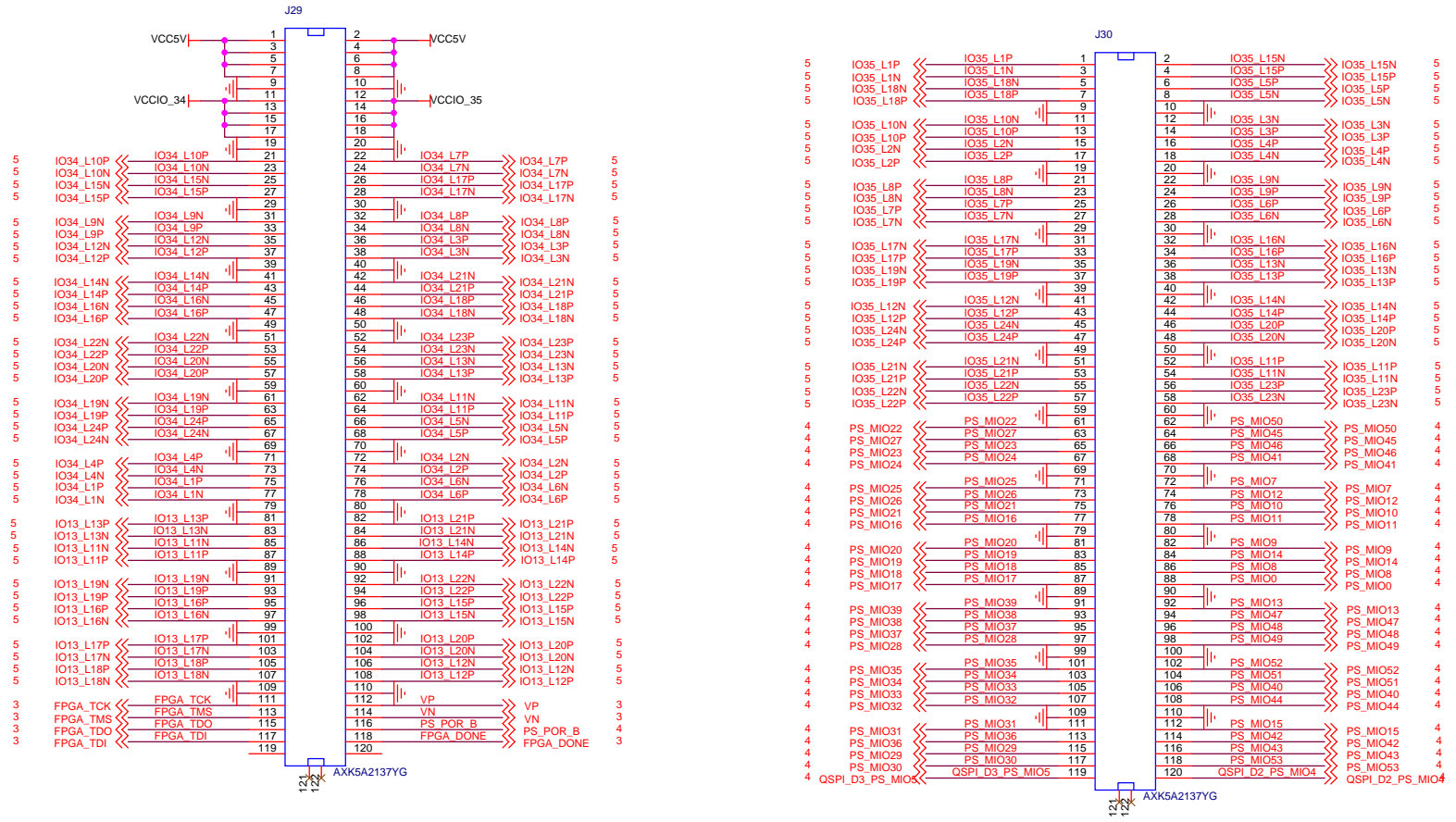




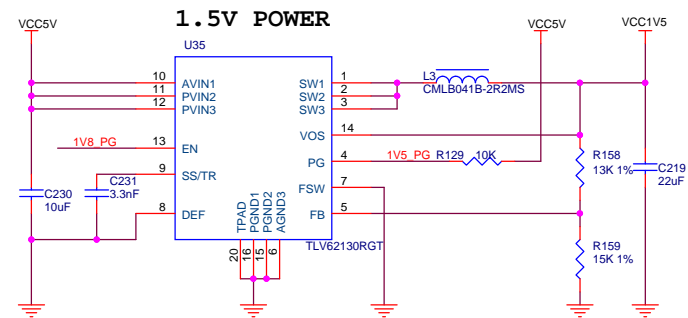
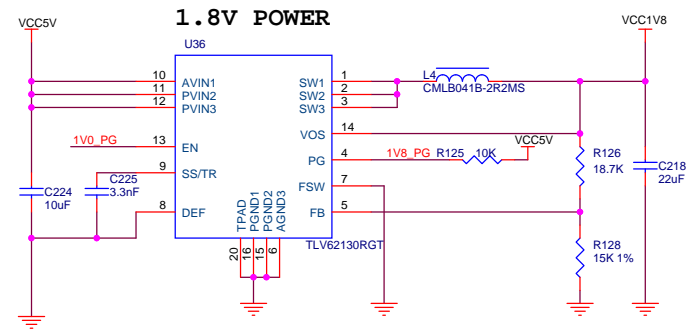
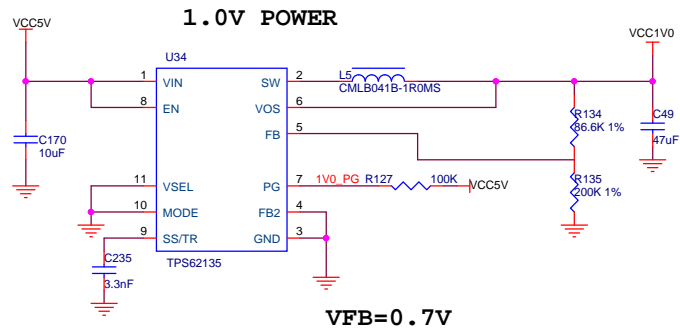
为了PCB走线方便, DDR3数据线组内 (DQS除外) 可以任意交换。
XILINX 的UG933文档的PAGE66有以下说明:



VCCIO34, VCCIO35的电源由底板提供, 不能超过3.3v, 上电顺序要求5v先供电, 然后再供VCCIO34和VCCIO35



BANK13的IO管脚只有AC7Z020的板子才有, AC7Z010的核心板无法使用这些IO



Power On Sequence:

1.0V -> 1.8V -> 1.5V -> 3.3V -> VCCIO

