ARM MPU AM335X CORE
ZCZ Package 15mm X 15mm

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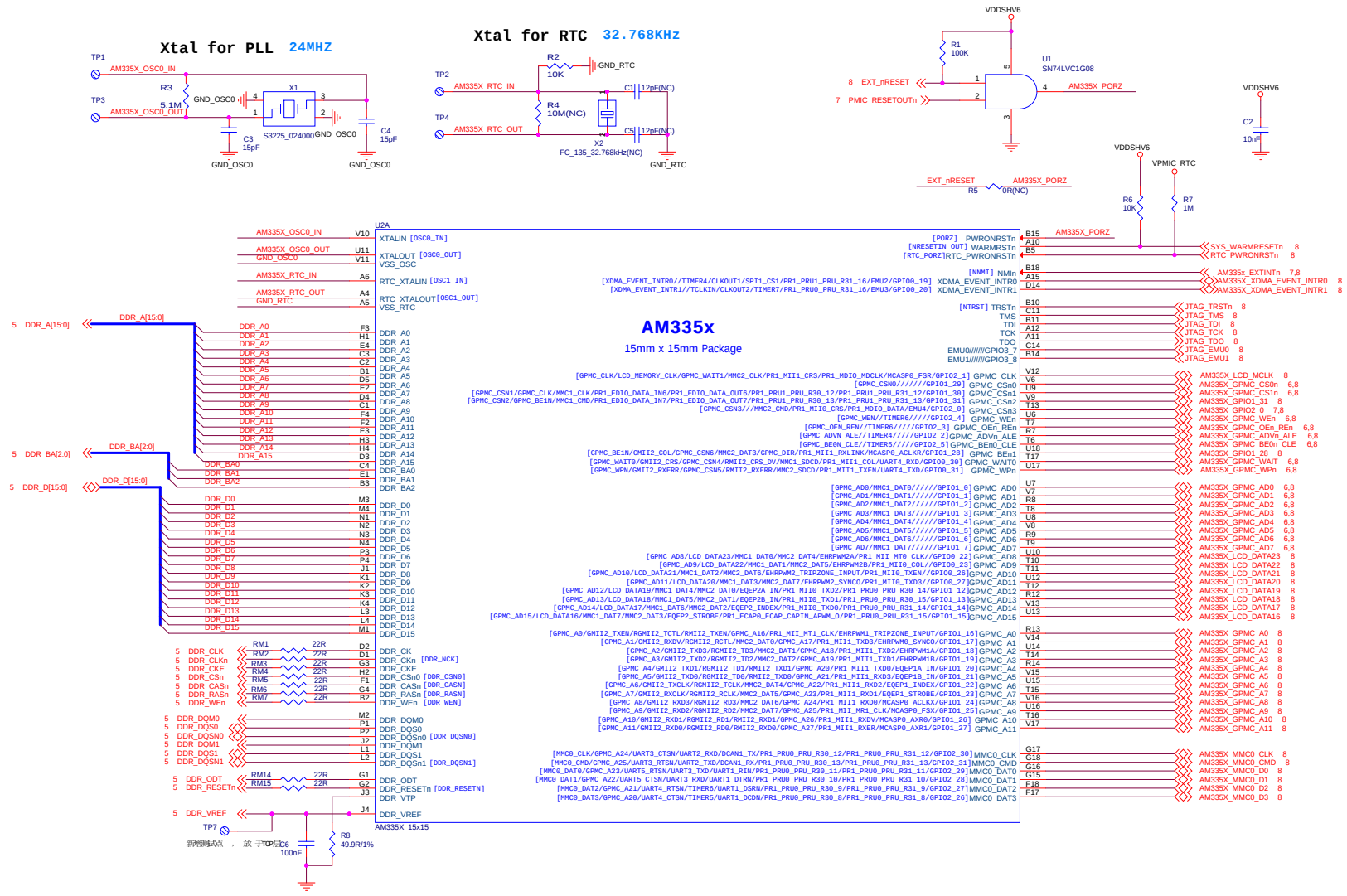
Xtal for PLL 24MHZ
Xtal for RTC 32.768KHz
AM335x
15mm x 15mm Package
AM335X_15x15
U2A
U1
SN74LVC1G08
VDDSHV6
VPMIC_RTC
TP1
TP2
TP3
TP4
TP7
R1 100K
R2 10K
R3 5.1M
R4 10M(NC)
R5 0R(NC)
R6 10K
R7 1M
R8 49.9R/1%
C1 12pF(NC)
C2 10nF
C3 15pF
C4 15pF
C5 12pF(NC)
C6 100nF
X1 S3225_024000
X2 FC_135_32.768kHz(NC)
GND_OSC0
GND_RTC
AM335X_OSC0_IN
AM335X_OSC0_OUT
AM335X_RTC_IN
AM335X_RTC_OUT
EXT_nRESET
PMIC_RESETOUTn
AM335X_PORZ
DDR_A[15:0]
DDR_BA[2:0]
DDR_D[15:0]
DDR_CLK
DDR_CLKn
DDR_CKE
DDR_CSn
DDR_CASn
DDR_RASn
DDR_WEn
DDR_DQM0
DDR_DQS0
DDR_DQSn0
DDR_DQM1
DDR_DQS1
DDR_DQSn1
DDR_ODT
DDR_RESETn
DDR_VREF
RM1 22R
RM2 22R
RM3 22R
RM4 22R
RM5 22R
RM6 22R
RM7 22R
RM14 22R
RM15 22R
JTAG_TRSTn
JTAG_TMS
JTAG_TDI
JTAG_TCK
JTAG_TDO
JTAG_EMU0
JTAG_EMU1
SYS_WARMRESETn
RTC_PWRONRSTn
AM335x_EXTINTn
AM335X_XDMA_EVENT_INTR0
AM335X_XDMA_EVENT_INTR1
AM335X_LCD_MCLK
AM335X_GPMC_CS0n
AM335X_GPMC_CS1n
AM335X_GPIO1_31
AM335X_GPIO2_0
AM335X_GPMC_WEn
AM335X_GPMC_OEn_REn
AM335X_GPMC_ADVn_ALE
AM335X_GPMC_BE0n_CLE
AM335X_GPIO1_28
AM335X_GPMC_WAIT
AM335X_GPMC_WPn
AM335X_LCD_DATA23
AM335X_LCD_DATA22
AM335X_LCD_DATA21
AM335X_LCD_DATA20
AM335X_LCD_DATA19
AM335X_LCD_DATA18
AM335X_LCD_DATA17
AM335X_LCD_DATA16
AM335X_GPMC_A0
AM335X_GPMC_A1
AM335X_GPMC_A2
AM335X_GPMC_A3
AM335X_GPMC_A4
AM335X_GPMC_A5
AM335X_GPMC_A6
AM335X_GPMC_A7
AM335X_GPMC_A8
AM335X_GPMC_A9
AM335X_GPMC_A10
AM335X_GPMC_A11
AM335X_MMC0_CLK
AM335X_MMC0_CMD
AM335X_MMC0_D0
AM335X_MMC0_D1
AM335X_MMC0_D2
AM335X_MMC0_D3
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AM335X
15mm x 15mm Package
U2B
AM335X_15x15
AM335X_TSXP
AM335X_TSXM
AM335X_TSYP
AM335X_TSYM
CL1 CL2 CL3 CL4
1nF 1nF 1nF 1nF
VDDA_ADC
R9 0R
C7 100nF
C8 1nF
GNDA_TSC
VREFP_ADC
PMIC_POWER_EN
EXT_WAKEUP
AIN0
AIN1
AIN2
AIN3
AIN4
AIN5
AIN6
AIN7
VREFP
VREFN
SPI0_SCLK [SPI0_SCLK/UART2_RXD/I2C2_SDA/EHRPWM0A/PR1_UART0_CTS_N/PR1_EDIO_SOF/EMU2/GPIO0_2]
SPI0_D0 [SPI0_D0/UART2_TXD/I2C2_SCL/EHRPWM0B/PR1_UART0_RTS_N/PR1_EDIO_LATCH_IN/EMU3/GPIO0_3]
SPI0_D1 [SPI0_D1/MMC1_SDWP/I2C1_SDA/EHRPWM0_TRIPZONE_INPUT/PR1_UART0_RXD/PR1_EDIO_DATA_IN0/PR1_EDIO_DATA_OUT0/GPIO0_4]
SPI0_CS0 [SPI0_CS0/MMC2_SDWP/I2C1_SCL/EHRPWM0_SYNCI/PR1_UART0_TXD/PR1_EDIO_DATA_IN1/PR1_EDIO_DATA_OUT1/GPIO0_5]
SPI0_CS1 [SPI0_CS1/UART3_RXD/ECAP1_IN_PWM1_OUT/MMC0_POW/XDMA_EVENT_INTR2/MMC0_SDCD/EMU4/GPIO0_6]
UART0_TXD [UART0_TXD/SPI1_CS1/DCAN0_RX/I2C2_SCL/ECAP1_IN_PWM1_OUT/PR1_PRU1_PRU_R30_15/PR1_PRU1_PRU_R31_15/GPIO1_11]
UART0_RXD [UART0_RXD/SPI1_CS0/DCAN0_TX/I2C2_SDA/ECAP2_IN_PWM2_OUT/PR1_PRU1_PRU_R30_14/PR1_PRU1_PRU_R31_14/GPIO1_10]
UART0_CTSn [UART0_CTSN/UART4_RXD/DCAN1_TX/I2C1_SDA/SPI1_D0/TIMER7/PR1_EDC_SYNC0_OUT/GPIO1_8]
UART0_RTSn [UART0_RTSN/UART4_TXD/DCAN1_RX/I2C1_SCL/SPI1_D1/SPI1_CS0/PR1_EDC_SYNC1_OUT/GPIO1_9]
UART1_TXD [UART1_TXD/MMC2_SDWP/DCAN1_RX/I2C1_SCL//PR1_UART0_TXD/PR1_PRU0_PRU_R31_16/GPIO0_15]
UART1_RXD [UART1_RXD/MMC1_SDWP/DCAN1_TX/I2C1_SDA//PR1_UART0_RXD/PR1_PRU1_PRU_R31_16/GPIO0_14]
UART1_CTSn [UART1_CTSN/TIMER6/DCAN0_TX/I2C2_SDA/SPI1_CS0/PR1_UART0_CTS_N/PR1_EDC_LATCH0_IN/GPIO0_12]
UART1_RTSn [UART1_RTSN/TIMER5/DCAN0_RX/I2C2_SCL/SPI1_CS1/PR1_UART0_RTS_N/PR1_EDC_LATCH1_IN/GPIO0_13]
I2C0_SCL [I2C0_SCL/TIMER7/UART2_RTSN/ECAP1_IN_PWM1_OUT////GPIO3_6]
I2C0_SDA [I2C0_SDA/TIMER4/UART2_CTSN/ECAP2_IN_PWM2_OUT////GPIO3_5]
USB0_DP
USB0_DM
USB0_CE
USB0_ID
USB0_DRVVBUS [USB0_DRVVBUS//////GPIO0_18]
USB0_VBUS
USB1_DP
USB1_DM
USB1_CE
USB1_ID
USB1_DRVVBUS[USB1_DRVVBUS//////GPIO3_13]
USB1_VBUS
ECAP0_IN_PWM0_OUT[ECAP0_IN_PWM0_OUT/UART3_TXD/SPI1_CS1/PR1_ECAP0_ECAP_CAPIN_APWM_O/SPI1_SCLK/MMC0_SDWP/XDMA_EVENT_INTR2/GPIO0_7]
VUSB_VBUS0
VUSB_VBUS1
R10 1.2K
R11 1.2K
R10 ,R11 - 0805Footprint,1/8W
[GMII1_TXCLK/UART2_RXD/RGMII1_TCLK/MMC0_DAT7/MMC1_DAT0/UART1_DCDN/MCASP0_ACLKX/GPIO3_9] MII1_TXCLK
[GMII1_TXD0/RMII1_TXD0/RGMII1_TD0/MCASP1_AXR3/MCASP1_ACLKR/EQEP0B_IN/MMC1_CLK/GPIO0_28] MII1_TXD0
[GMII1_TXD1/RMII1_TXD1/RGMII1_TD1/MCASP1_FSR/MCASP1_AXR1/EQEP0A_IN/MMC1_CMD/GPIO0_21] MII1_TXD1
[GMII1_TXD2/DCAN0_RX/RGMII1_TD2/UART4_TXD/MCASP1_AXR0/MMC2_DAT2/MCASP0_AHCLKX/GPIO0_17] MII1_TXD2
[GMII1_TXD3/DCAN0_TX/RGMII1_TD3/UART4_RXD/MCASP1_FSX/MMC2_DAT1/MCASP0_FSR/GPIO0_16] MII1_TXD3
[GMII1_TXEN/RMII1_TXEN/RGMII1_TCTL/TIMER4/MCASP1_AXR0/EQEP0_INDEX/MMC2_CMD/GPIO3_3] MII1_TXEN
[GMII1_CRS/RMII1_CRS_DV/SPI1_D0/I2C1_SDA/MCASP1_ACLKX/UART5_CTSN/UART2_RXD/GPIO3_1] MII1_CRS
[GMII1_COL/RMII2_REFCLK/SPI1_SCLK/UART5_RXD/MCASP1_AXR2/MMC2_DAT3/MCASP0_AXR2/GPIO3_0] MII1_COL
[GMII1_RXCLK/UART2_TXD/RGMII1_RCLK/MMC0_DAT6/MMC1_DAT1/UART1_DSRN/MCASP0_FSX/GPIO3_10] MII1_RXCLK
[GMII1_RXD0/RMII1_RXD0/RGMII1_RD0/MCASP1_AHCLKX/MCASP1_AHCLKR/MCASP1_ACLKR/MCASP0_AXR3/GPIO2_21] MII1_RXD0
[GMII1_RXD1/RMII1_RXD1/RGMII1_RD1/MCASP1_AXR3/MCASP1_FSR/EQEP0_STROBE/MMC2_CLK/GPIO2_20] MII1_RXD1
[GMII1_RXD2/UART3_TXD/RGMII1_RD2/MMC0_DAT4/MMC1_DAT3/UART1_RIN/MCASP0_AXR1/GPIO2_19] MII1_RXD2
[GMII1_RXD3/UART3_RXD/RGMII1_RD3/MMC0_DAT5/MMC1_DAT2/UART1_DTRN/MCASP0_AXR0/GPIO2_18] MII1_RXD3
[GMII1_RXERR/RMII1_RXERR/SPI1_D1/I2C1_SCL/MCASP1_FSX/UART5_RTSN/UART2_TXD/GPIO3_2] MII1_RXERR
[GMII1_RXDV/LCD_MEMORY_CLK/RGMII1_RCTL/UART5_TXD/MCASP1_ACLKX/MMC2_DAT0/MCASP0_ACLKR/GPIO3_4] MII1_RXDV
[RMII1_REFCLK/XDMA_EVENT_INTR2/SPI1_CS0/UART5_TXD/MCASP1_AXR3/MMC0_POW/MCASP1_AHCLKX/GPIO0_29] MII1_REFCLK
[MDIO_CLK/TIMER5/UART5_TXD/UART3_RTSN/MMC0_SDWP/MMC1_CLK/MMC2_CLK/GPIO0_1] MDIO_CLK
[MDIO_DATA/TIMER6/UART5_RXD/UART3_CTSN/MMC0_SDCD/MMC1_CMD/MMC2_CMD/GPIO0_0] MDIO_DATA
[LCD_DATA0/GPMC_A0/PR1_MII_MT0_CLK/EHRPWM2A//PR1_PRU1_PRU_R30_0/PR1_PRU1_PRU_R31_0/GPIO2_6] LCD_DATA0
[LCD_DATA1/GPMC_A1/PR1_MII0_TXEN/EHRPWM2B//PR1_PRU1_PRU_R30_1/PR1_PRU1_PRU_R31_1/GPIO2_7] LCD_DATA1
[LCD_DATA2/GPMC_A2/PR1_MII0_TXD3/EHRPWM2_TRIPZONE_INPUT//PR1_PRU1_PRU_R30_2/PR1_PRU1_PRU_R31_2/GPIO2_8] LCD_DATA2
[LCD_DATA3/GPMC_A3/PR1_MII0_TXD2/EHRPWM2_SYNCI_O//PR1_PRU1_PRU_R30_3/PR1_PRU1_PRU_R31_3/GPIO2_9] LCD_DATA3
[LCD_DATA4/GPMC_A4/PR1_MII0_TXD1/EQEP2A_IN//PR1_PRU1_PRU_R30_4/PR1_PRU1_PRU_R31_4/GPIO2_10] LCD_DATA4
[LCD_DATA5/GPMC_A5/PR1_MII0_TXD0/EQEP2B_IN//PR1_PRU1_PRU_R30_5/PR1_PRU1_PRU_R31_5/GPIO2_11] LCD_DATA5
[LCD_DATA6/GPMC_A6/PR1_EDIO_DATA_IN6/EQEP2_INDEX/PR1_EDIO_DATA_OUT6/PR1_PRU1_PRU_R30_6/PR1_PRU1_PRU_R31_6/GPIO2_12] LCD_DATA6
[LCD_DATA7/GPMC_A7/PR1_EDIO_DATA_IN7/EQEP2_STROBE/PR1_EDIO_DATA_OUT7/PR1_PRU1_PRU_R30_7/PR1_PRU1_PRU_R31_7/GPIO2_13] LCD_DATA7
[LCD_DATA8/GPMC_A12/EHRPWM1_TRIPZONE_INPUT/MCASP0_ACLKX/UART5_TXD/PR1_MII0_RXD3/UART2_CTSN/GPIO2_14] LCD_DATA8
[LCD_DATA9/GPMC_A13/EHRPWM1_SYNCO/MCASP0_FSX/UART5_RXD/PR1_MII0_RXD2/UART2_RTSN/GPIO2_15] LCD_DATA9
[LCD_DATA10/GPMC_A14/EHRPWM1A/MCASP0_AXR0//PR1_MII0_RXD1/UART3_CTSN/GPIO2_16] LCD_DATA10
[LCD_DATA11/GPMC_A15/EHRPWM1B/MCASP0_AHCLKR/MCASP0_AXR2/PR1_MII0_RXD0/UART3_RTSN/GPIO2_17] LCD_DATA11
[LCD_DATA12/GPMC_A16/EQEP1A_IN/MCASP0_ACLKR/MCASP0_AXR2/PR1_MII0_RXLINK/UART4_CTSN/GPIO0_8] CD_DATA12
[LCD_DATA13/GPMC_A17/EQEP1B_IN/MCASP0_FSR/MCASP0_AXR3/PR1_MII0_RXER/UART4_RTSN/GPIO0_9] LCD_DATA13
[LCD_DATA14/GPMC_A18/EQEP1_INDEX/MCASP0_AXR1/UART5_RXD/PR1_MII_MR0_CLK/UART5_CTSN/GPIO0_10] LCD_DATA14
[LCD_DATA15/GPMC_A19/EQEP1_STROBE/MCASP0_AHCLKX/MCASP0_AXR3/PR1_MII0_RXDV/UART5_RTSN/GPIO0_11] LCD_DATA15
[LCD_PCLK/GPMC_A10/PR1_MII0_CRS/PR1_EDIO_DATA_IN4/PR1_EDIO_DATA_OUT4/PR1_PRU1_PRU_R30_10/PR1_PRU1_PRU_R31_10/GPIO2_24] LCD_PCLK
[LCD_VSYNC/GPMC_A8//PR1_EDIO_DATA_IN2/PR1_EDIO_DATA_OUT2/PR1_PRU1_PRU_R30_8/PR1_PRU1_PRU_R31_8/GPIO2_22] LCD_VSYNC
[LCD_HSYNC/GPMC_A9//PR1_EDIO_DATA_IN3/PR1_EDIO_DATA_OUT3/PR1_PRU1_PRU_R30_9/PR1_PRU1_PRU_R31_9/GPIO2_23] LCD_HSYNC
[LCD_AC_BIAS_EN/GPMC_A11/PR1_MII1_CRS/PR1_EDIO_DATA_IN5/PR1_EDIO_DATA_OUT5/PR1_PRU1_PRU_R30_11/PR1_PRU1_PRU_R31_11/GPIO2_25] LCD_AC_BIAS_EN
[MCASP0_AHCLKX/EQEP0_STROBE/MCASP0_AXR3/MCASP1_AXR1/EMU4/PR1_PRU0_PRU_R30_7/PR1_PRU0_PRU_R31_7/GPIO3_21] MCASP0_AHCLKX
[MCASP0_ACLKX/EHRPWM0A//SPI1_SCLK/MMC0_SDCD/PR1_PRU0_PRU_R30_0/PR1_PRU0_PRU_R31_0/GPIO3_14] MCASP0_ACLKX
[MCASP0_FSX/EHRPWM0B//SPI1_D0/MMC1_SDCD/PR1_PRU0_PRU_R30_1/PR1_PRU0_PRU_R31_1/GPIO3_15] MCASP0_FSX
[MCASP0_AXR0/EHRPWM0_TRIPZONE_INPUT//SPI1_D1/MMC2_SDCD/PR1_PRU0_PRU_R30_2/PR1_PRU0_PRU_R31_2/GPIO3_16] MCASP0_AXR0
[MCASP0_AHCLKR/EHRPWM0_SYNCI_O/MCASP0_AXR2/SPI1_CS0/ECAP2_IN_PWM2_OUT/PR1_PRU0_PRU_R30_3/PR1_PRU0_PRU_R31_3/GPIO3_17] MCASP0_AHCLKR
[MCASP0_ACLKR/EQEP0A_IN/MCASP0_AXR2/MCASP1_ACLKX/MMC0_SDWP/PR1_PRU0_PRU_R30_4/PR1_PRU0_PRU_R31_4/GPIO3_18] MCASP0_ACLKR
[MCASP0_FSR/EQEP0B_IN/MCASP0_AXR3/MCASP1_FSX/EMU2/PR1_PRU0_PRU_R30_5/PR1_PRU0_PRU_R31_5/GPIO3_19] MCASP0_FSR
[MCASP0_AXR1/EQEP0_INDEX//MCASP1_AXR0/EMU3/PR1_PRU0_PRU_R30_6/PR1_PRU0_PRU_R31_6/GPIO3_20] MCASP0_AXR1
AM335X_GMII1_TXCLK 8
AM335X_GMII1_TXD0 8
AM335X_GMII1_TXD1 8
AM335X_GMII1_TXD2 8
AM335X_GMII1_TXD3 8
AM335X_GMII1_TXEN 8
AM335X_GMII1_CRS 8
AM335X_GMII1_COL 8
AM335X_GMII1_RXCLK 8
AM335X_GMII1_RXD0 8
AM335X_GMII1_RXD1 8
AM335X_GMII1_RXD2 8
AM335X_GMII1_RXD3 8
AM335X_GMII1_RXERR 8
AM335X_GMII1_RXDV 8
AM335X_SPI1_CS0 8
AM335X_GMII1_MDIO_CLK 8
AM335X_GMII1_MDIO_DATA 8
AM335X_LCD_DATA0 8
AM335X_LCD_DATA1 8
AM335X_LCD_DATA2 8
AM335X_LCD_DATA3 8
AM335X_LCD_DATA4 8
AM335X_LCD_DATA5 8
AM335X_LCD_DATA6 8
AM335X_LCD_DATA7 8
AM335X_LCD_DATA8 8
AM335X_LCD_DATA9 8
AM335X_LCD_DATA10 8
AM335X_LCD_DATA11 8
AM335X_LCD_DATA12 8
AM335X_LCD_DATA13 8
AM335X_LCD_DATA14 8
AM335X_LCD_DATA15 8
AM335X_LCD_PCLK 8
AM335X_LCD_VSYNC 8
AM335X_LCD_HSYNC 8
AM335X_LCD_AC_BIAS_EN 8
AM335X_MCASP1_AXR1 8
AM335X_SPI1_SCLK 8
AM335X_SPI1_D0 8
AM335X_SPI1_D1 8
AM335X_ECAP2_IN_PWM2_OUT 8
AM335X_MCASP1_ACLKX 8
AM335X_MCASP1_FSX 8
AM335X_MCASP1_AXR0 8
VDDSHV6
R12 1.2K
R13 1.2K
R14 4.7K
R15 4.7K
R16 4.7K
R17 4.7K
AM335X_I2C0_SCL
AM335X_I2C0_SDA
AM335X_I2C1_SCL
AM335X_I2C1_SDA
AM335X_I2C2_SCL
AM335X_I2C2_SDA
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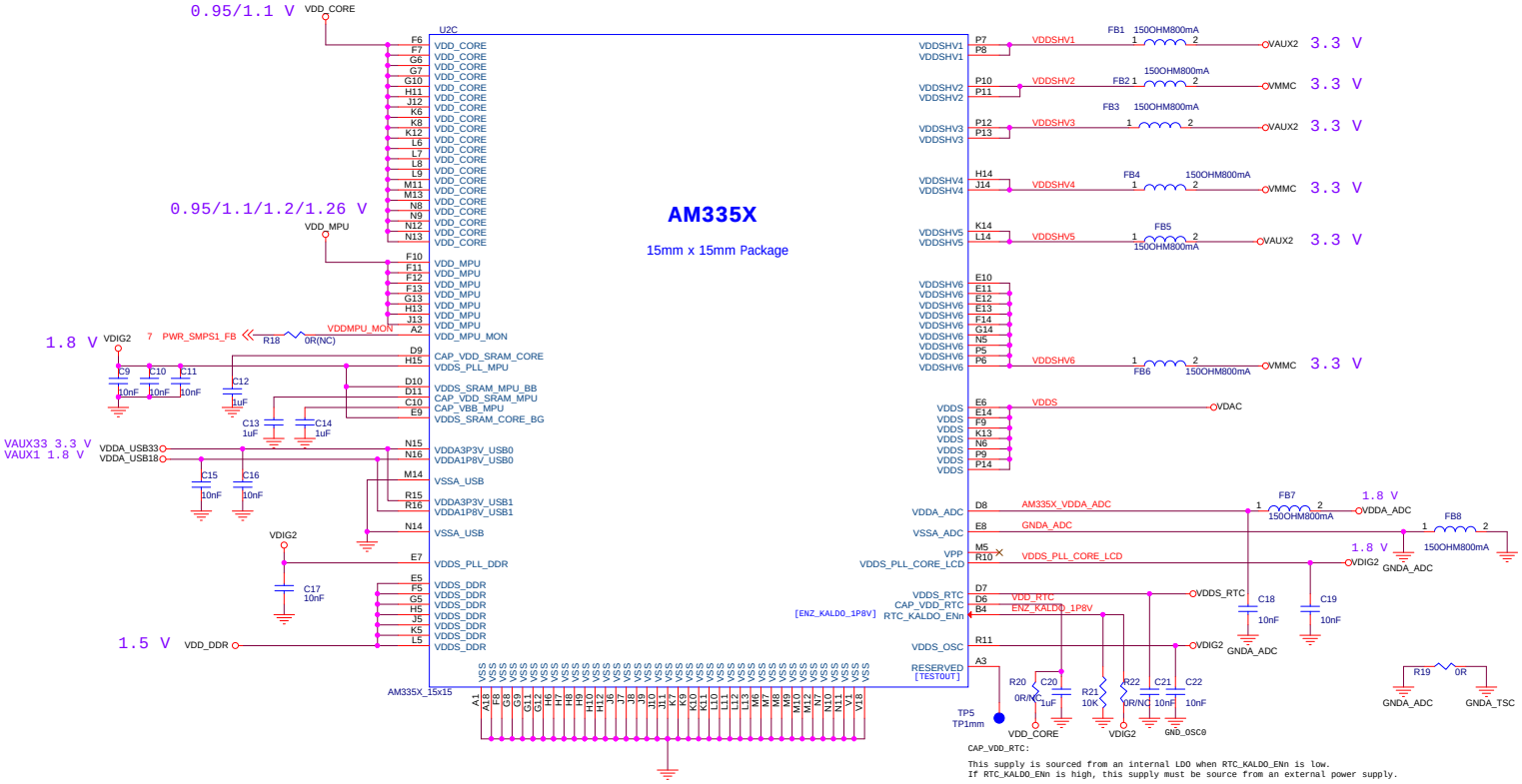

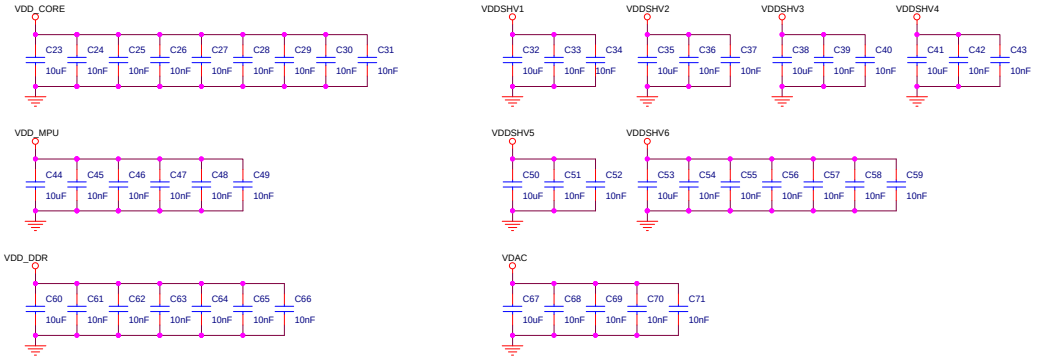

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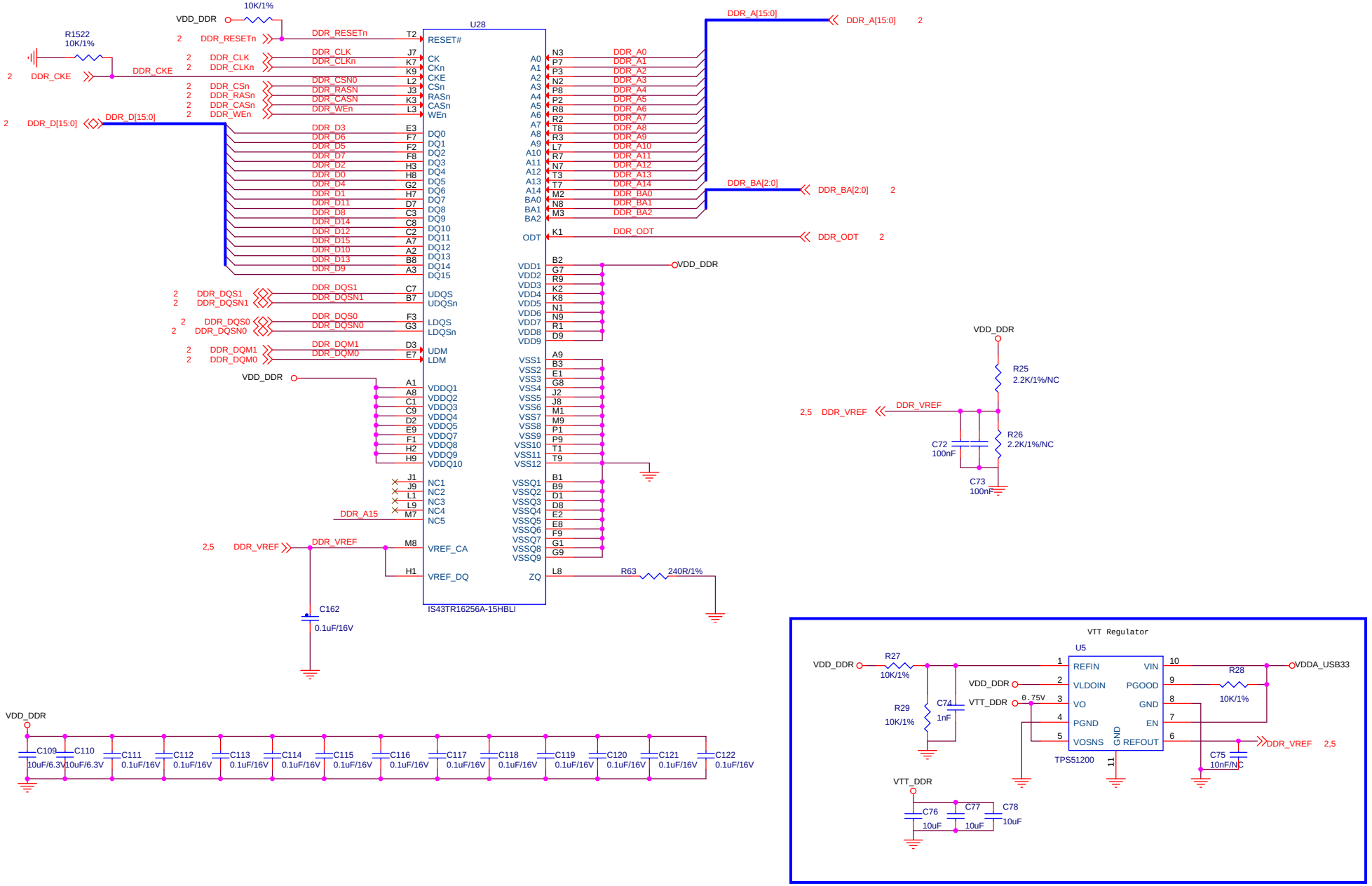
DDR3 SDRAM



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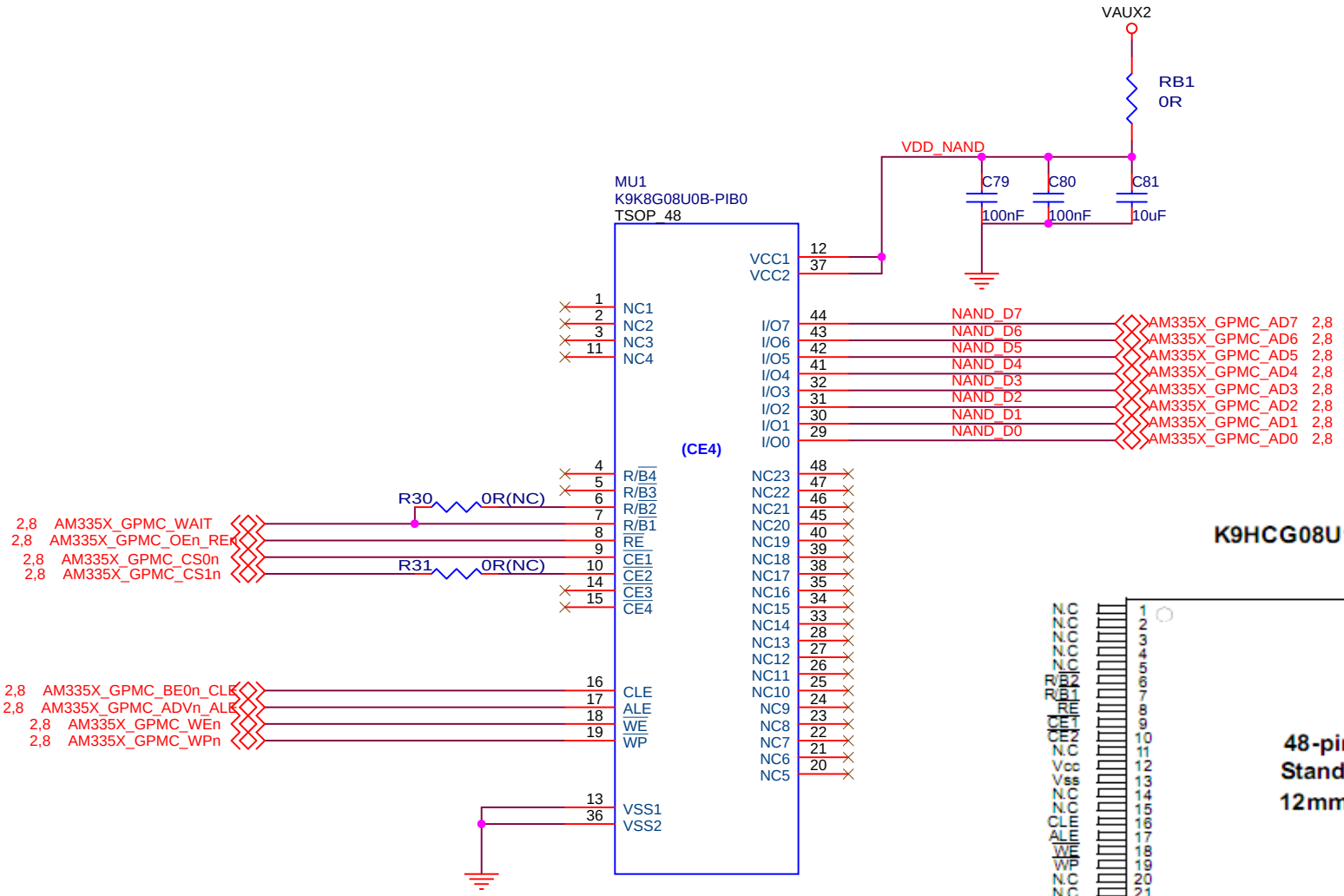

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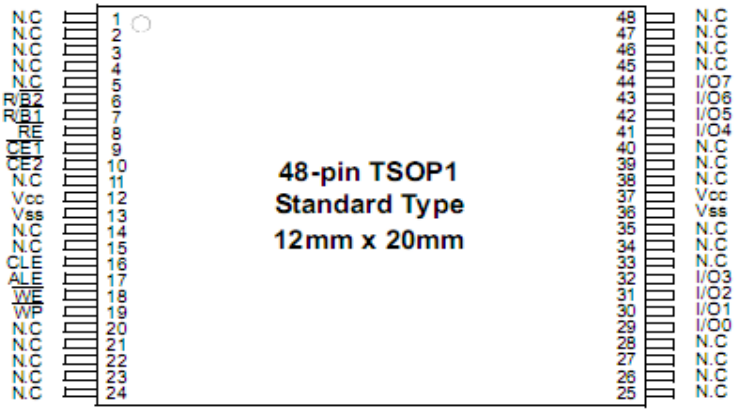

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Table 3-5. Operating Performance Points for ZCZ Package[1]

OPP	VDD_MPU[2]	VDD_CORE[2]	ARM (A8)	DDR3	DDR2	mDDR	L3/L4
Turbo	1.26 V ±4%	1.1 V ±4%	720 MHz	303 MHz	200 MHz	180 MHz	200/100 MHz
OPP120	1.2 V ±4%	1.1 V ±4%	600 MHz	303 MHz	200 MHz	180 MHz	200/100 MHz
OPP100	1.1 V ±4%	1.1 V ±4%	500 MHz	303 MHz	200 MHz	180 MHz	200/100 MHz
OPP50	0.95 V ±4%	0.95 V ±4%	275 MHz	-	125 MHz	90 MHz	100/50 MHz

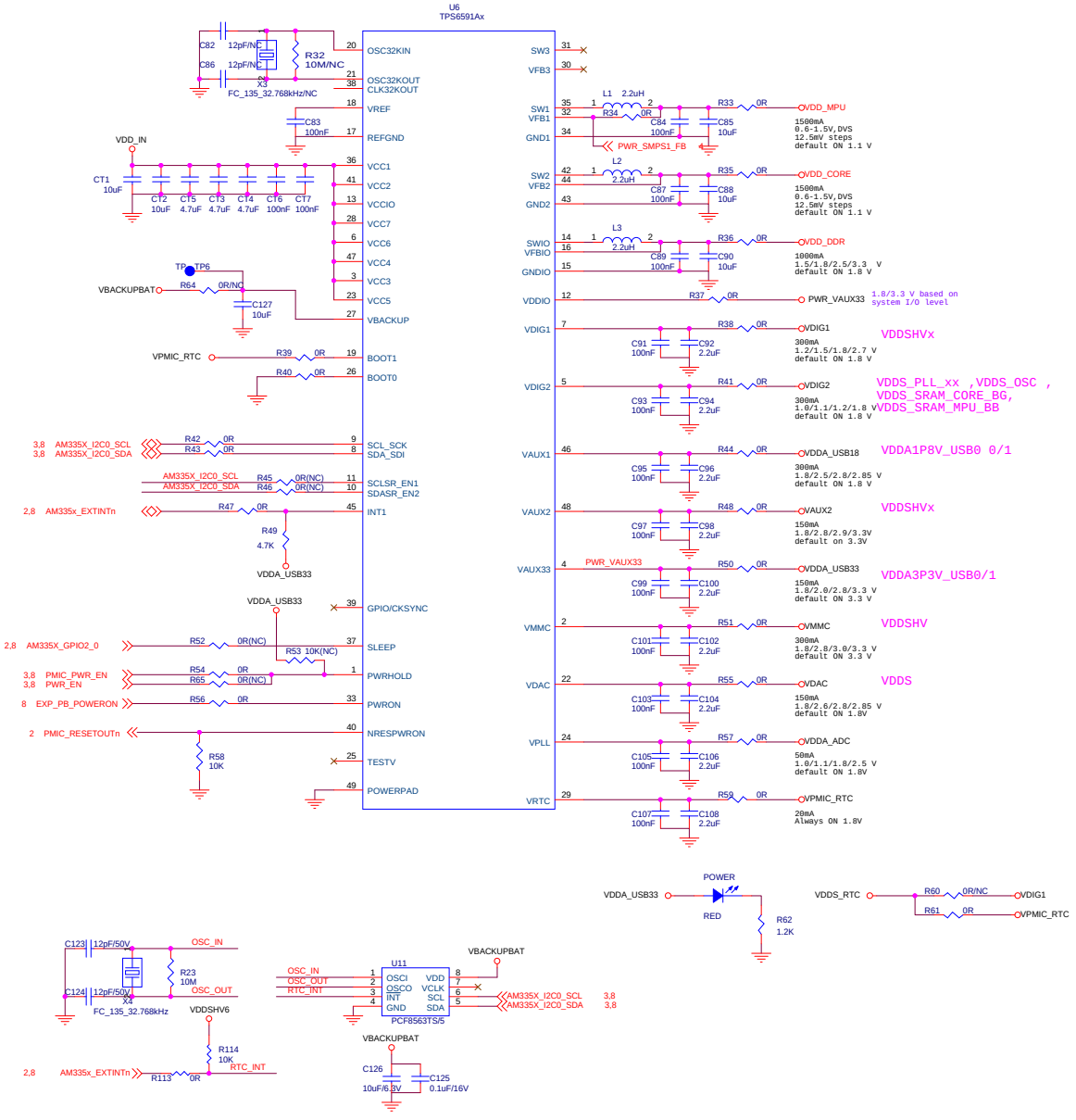

Table 3-4. Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
SUPPLY NAME	DESCRIPTION				
VDD_CORE	Supply voltage range for core domain	1.06	1.1	1.15	V
VDD_MPU[1]	Supply voltage range for MPU domain; TURBO	1.21	1.26	1.31	V
	Supply voltage range for MPU domain; OPP120	1.15	1.2	1.25	
	Supply voltage range for MPU domain; OPP100	1.06	1.1	1.15	
	Supply voltage range for MPU domain; OPP50	0.91	0.95	0.99	
CAP_VDD_RTC[2]	Supply voltage range for RTC domain input/LDO output	1.06	1.1	1.15	V
VDDS_RTC	Supply voltage range for RTC domain	1.71	1.8	1.89	V
VDDS_DDR	Supply voltage range for DDR IO domain (DDR2)	1.71	1.8	1.89	V
	Supply voltage range for DDR IO domain (DDR3)	1.43	1.5	1.58	
VDDS[3]	Supply voltage range for all Dual Voltage IO domains	1.71	1.8	1.89	V
VDDS_SRAM_CORE_BG	Supply voltage range for Core SRAM LDOs, Analog	1.71	1.8	1.89	V
VDDS_SRAM_MPU_BB	Supply voltage range for MPU SRAM LDOs, Analog	1.71	1.8	1.89	V
VDDS_PLL_DDR	Supply voltage range for DPLL DDR, Analog	1.71	1.8	1.89	V
VDDS_PLL_CORE_LCD	Supply voltage range for DPLL CORE and LCD, Analog	1.71	1.8	1.89	V
VDDS_PLL_MPU	Supply voltage range for DPLL MPU, Analog	1.71	1.8	1.89	V
VDDS_OSC	Supply voltage range for system oscillator IO's, Analog	1.71	1.8	1.89	V
VDDA1P8V_USB0	Supply voltage range for USB PHY, Analog, 1.8V	1.71	1.8	1.89	V
VDDA1P8V_USB1[4]	Supply voltage range for USB PHY, Analog, 1.8V	1.71	1.8	1.89	V
VDDA3P3V_USB0	Supply voltage range for USB PHY, Analog, 3.3V	3.14	3.3	3.47	V
VDDA3P3V_USB1[4]	Supply voltage range for USB PHY, Analog, 3.3V	3.14	3.3	3.47	V
VDDA_ADC	Supply voltage range for ADC, Analog	1.71	1.8	1.89	V
VDDSHV1	Supply voltage range for Dual Voltage IO domain (1.8-V operation)	1.71	1.8	1.89	V
VDDSHV2[4]	Supply voltage range for Dual Voltage IO domain (1.8-V operation)	1.71	1.8	1.89	V
VDDSHV3[4]	Supply voltage range for Dual Voltage IO domain (1.8-V operation)	1.71	1.8	1.89	V
VDDSHV4	Supply voltage range for Dual Voltage IO domain (1.8-V operation)	1.71	1.8	1.89	V
VDDSHV5	Supply voltage range for Dual Voltage IO domain (1.8-V operation)	1.71	1.8	1.89	V
VDDSHV6	Supply voltage range for Dual Voltage IO domain (1.8-V operation)	1.71	1.8	1.89	V
VDDSHV1	Supply voltage range for Dual Voltage IO domain (3.3-V operation)	3.14	3.3	3.47	V
VDDSHV2[4]	Supply voltage range for Dual Voltage IO domain (3.3-V operation)	3.14	3.3	3.47	V
VDDSHV3[4]	Supply voltage range for Dual Voltage IO domain (3.3-V operation)	3.14	3.3	3.47	V
VDDSHV4	Supply voltage range for Dual Voltage IO domain (3.3-V operation)	3.14	3.3	3.47	V
VDDSHV5	Supply voltage range for Dual Voltage IO domain (3.3-V operation)	3.14	3.3	3.47	V
VDDSHV6	Supply voltage range for Dual Voltage IO domain (3.3-V operation)	3.14	3.3	3.47	V
DDR_VREF	Voltage range for DDR SSTL/HSTL reference input (DDR2/DDR3)	0.49*VDDS_DDR	0.50*VDDS_DDR	0.51*VDDS_DDR	V
USB0_VBUS	Voltage range for USB VBUS comparator input	0		5	V
USB1_VBUS[4]	Voltage range for USB VBUS comparator input	0		5	V
USB0_ID	Voltage range for the USB ID input	1.71	1.8	1.89	V
USB1_ID[4]	Voltage range for the USB ID input	1.71	1.8	1.89	V

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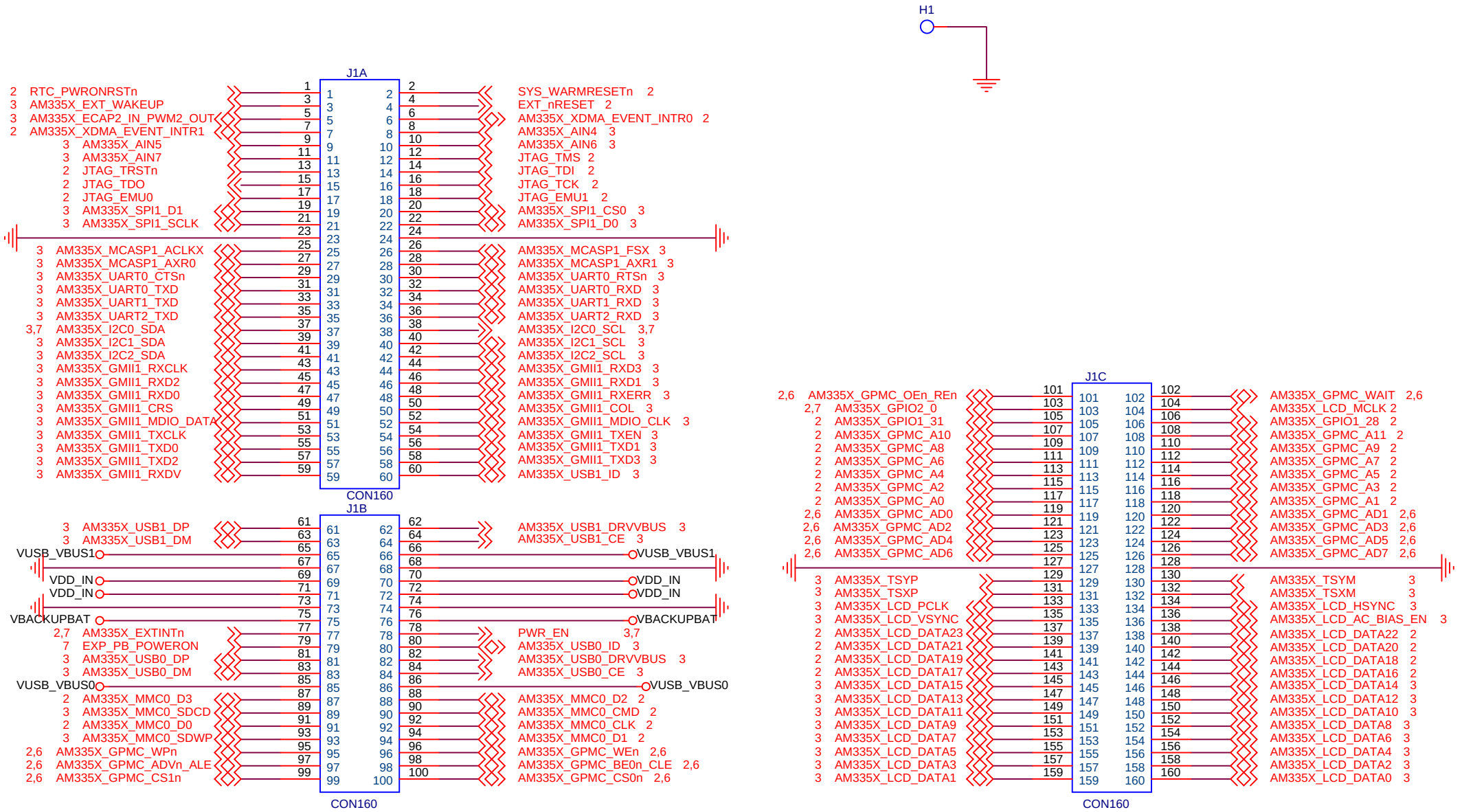

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