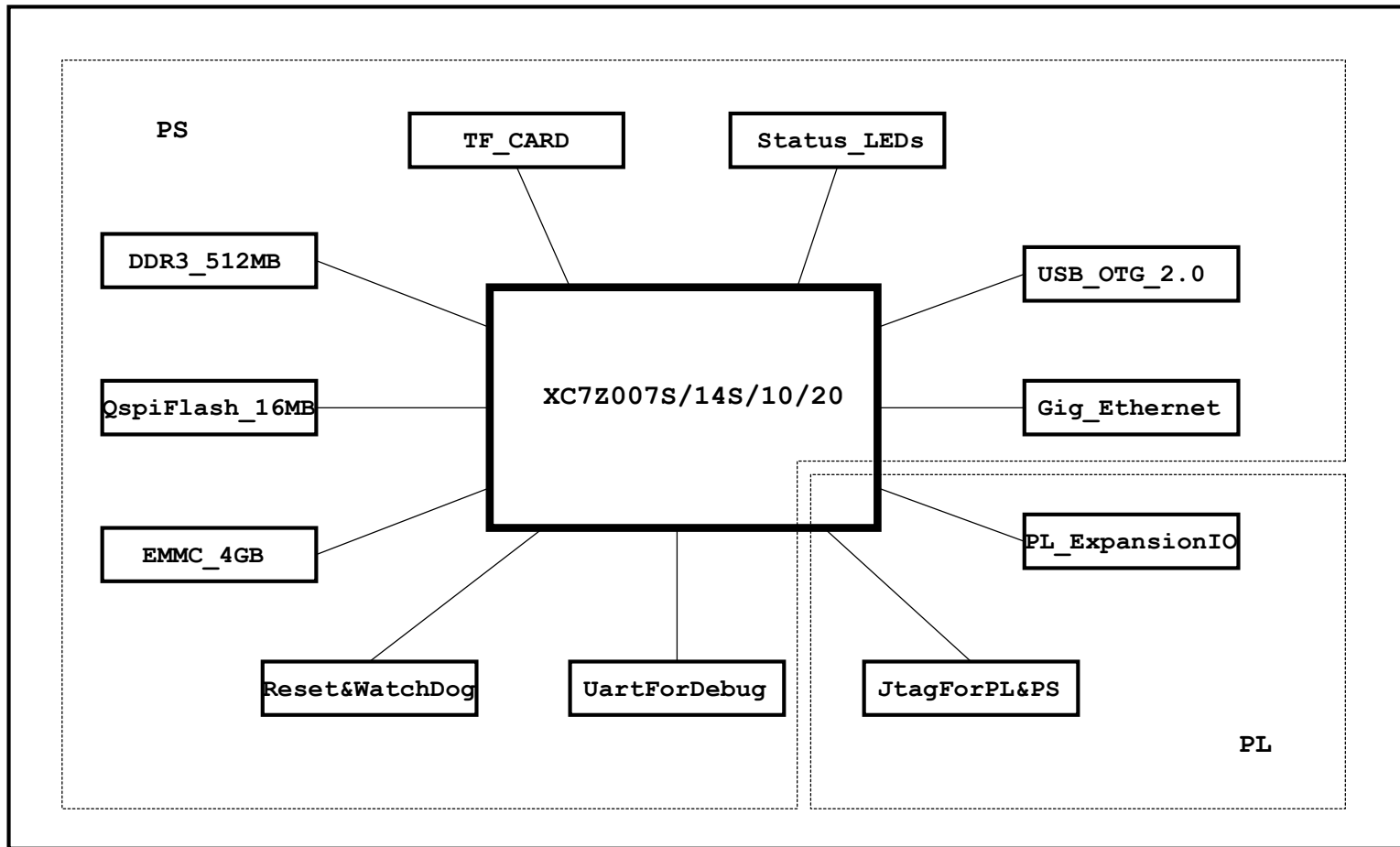


| REV | Description | DATE | BY |
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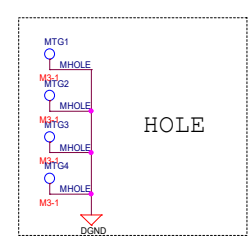
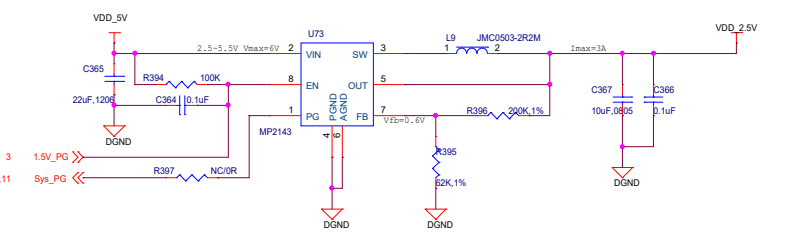
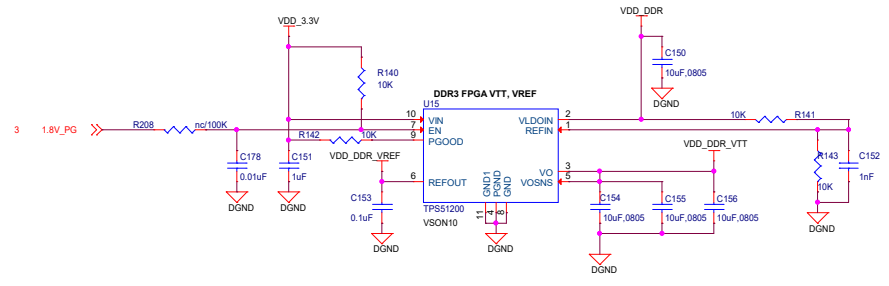
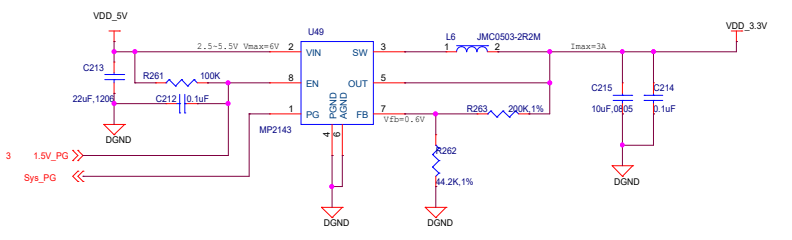
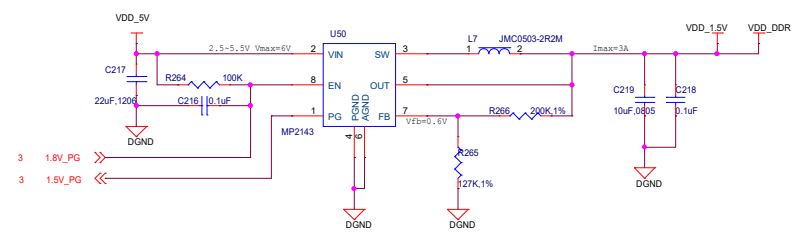
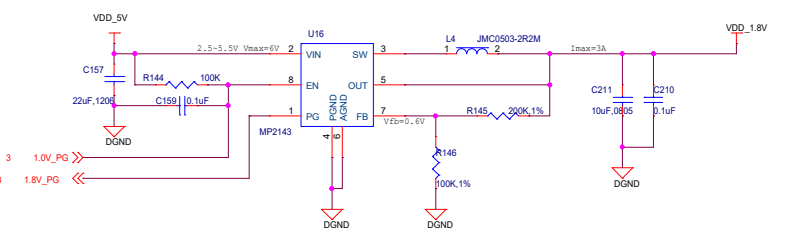
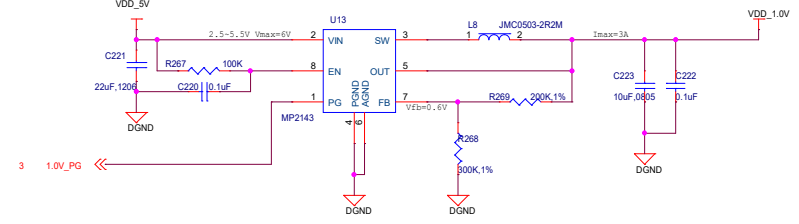
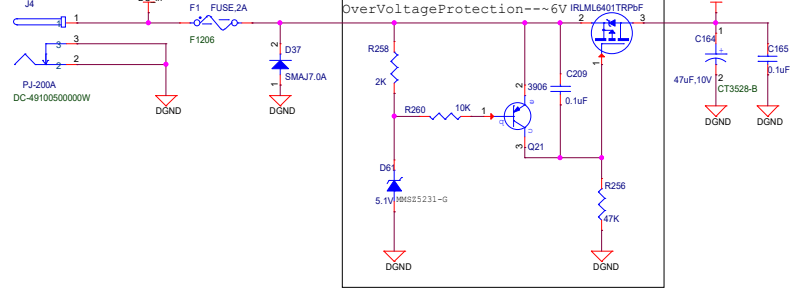
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|----------|------------------------------|
| 1 | TITLE PAGE |
| 2 | BLOCK |
| 3 | DCin & PowerSystem |
| 4 | Z7007S/10_POWER |
| 5 | Z7007S/10_PL |
| 6 | Z7007S/10_PS |
| 7 | DDR3 MEMORY |
| 8 | QspiFlash & Emmc & TF |
| 9 | 10/100/1000 ETHERNET |
| 10 | USB OTG |
| 11 | WatchDog & Reset |
| 12 | Jtag & DebugUart & StatusLed |
| 13 | Exp Conn |
| | |
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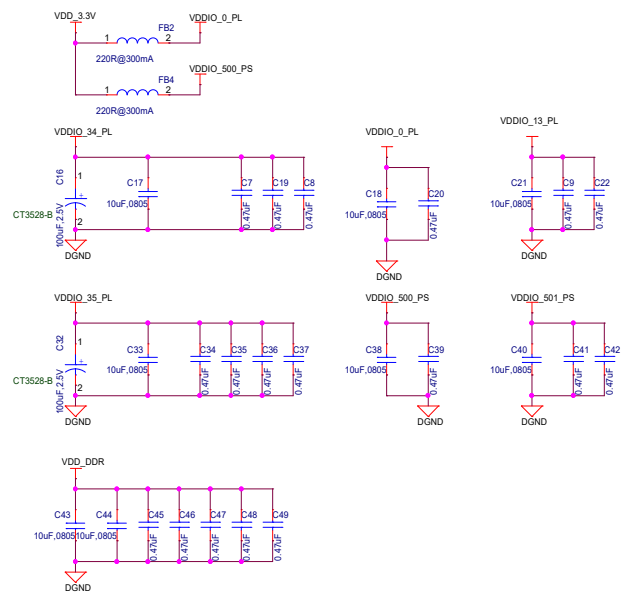
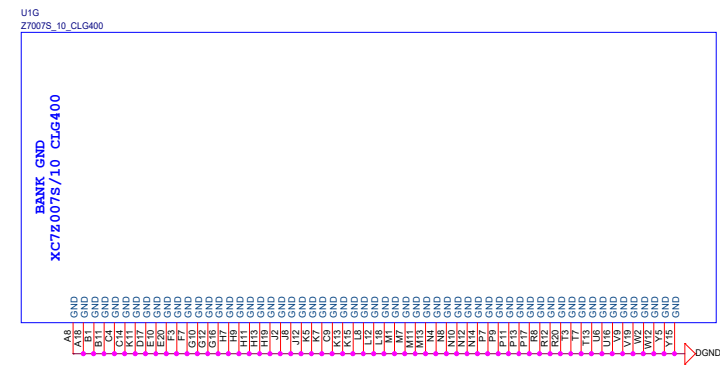
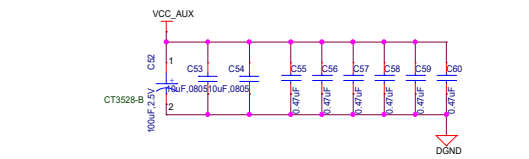
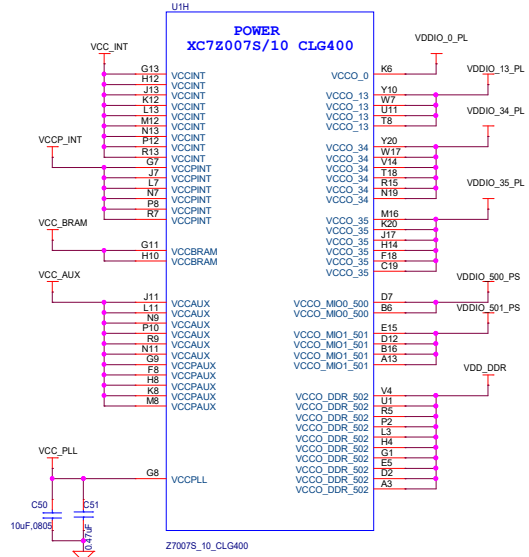
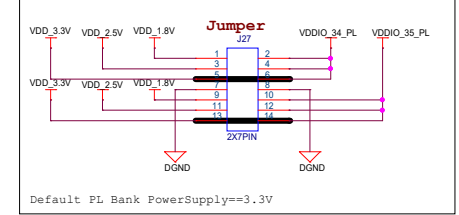
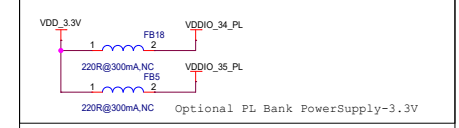
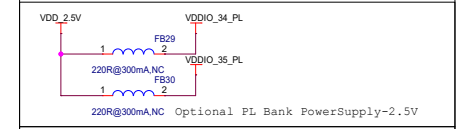
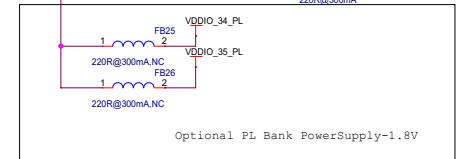
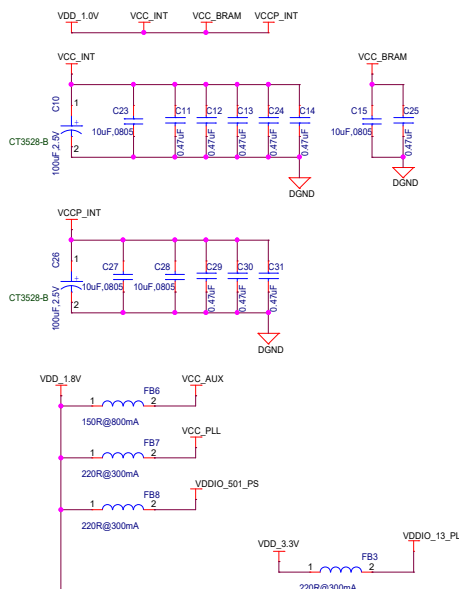
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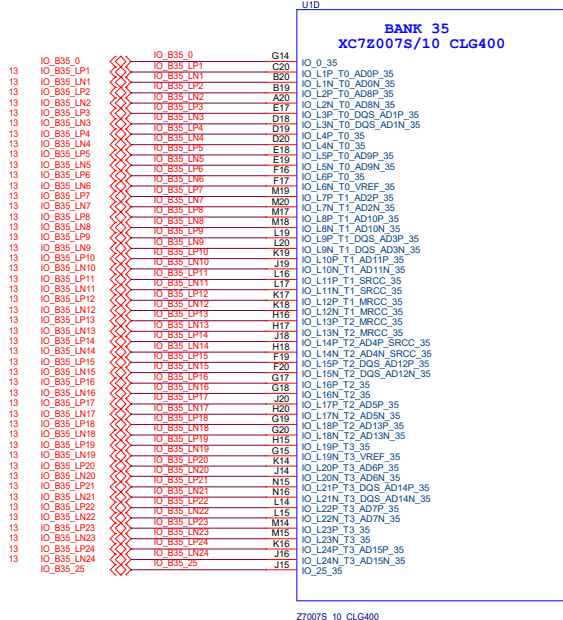
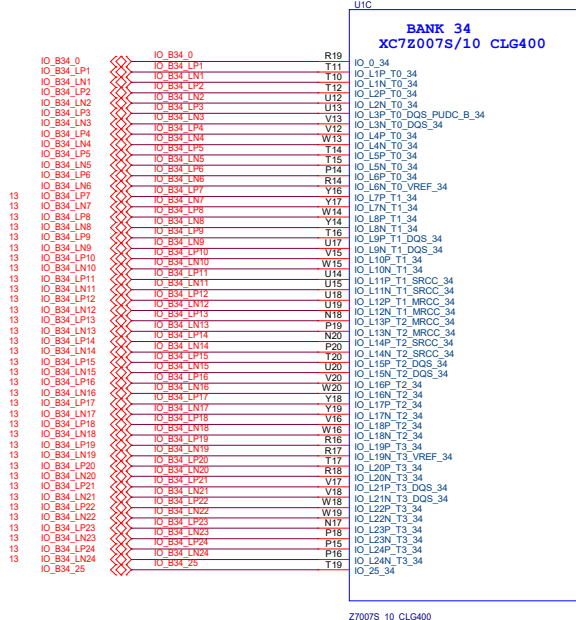
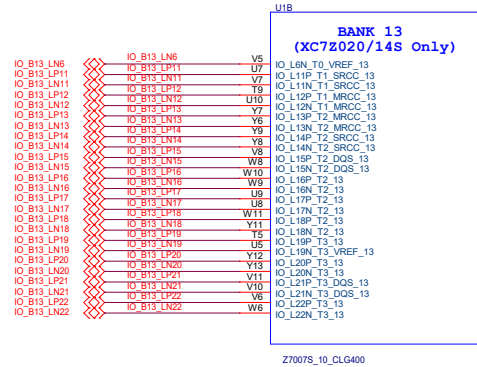
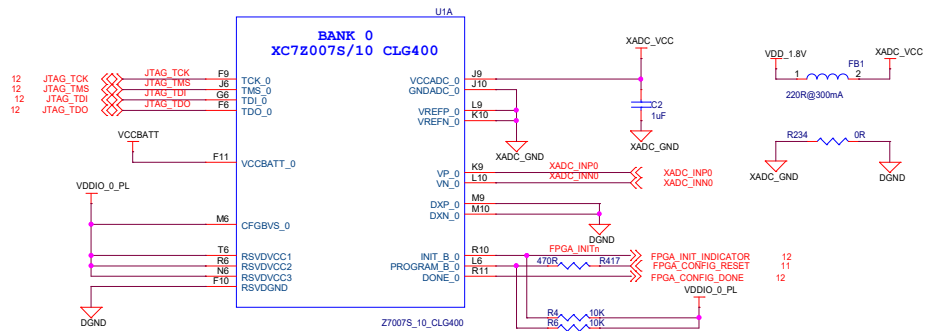


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DC_IN 5vInput







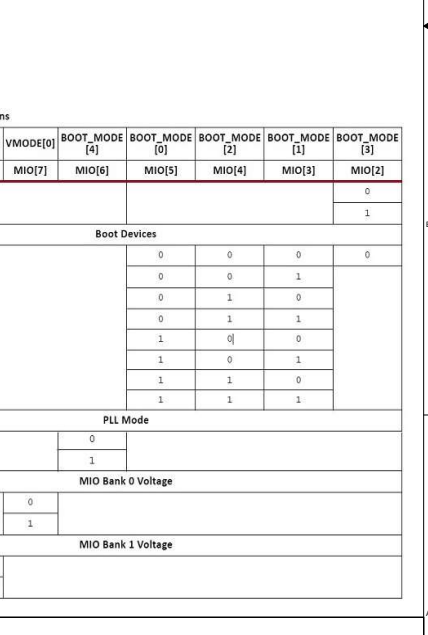
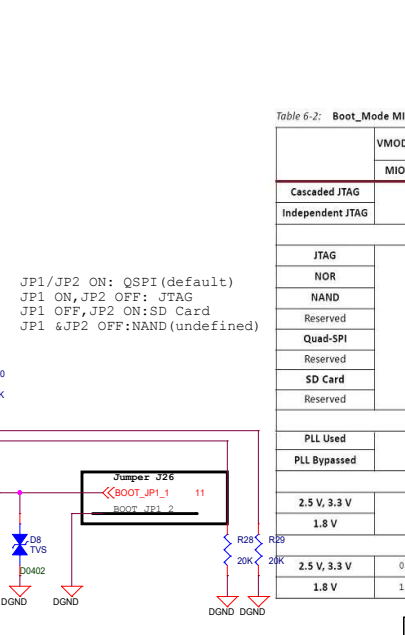
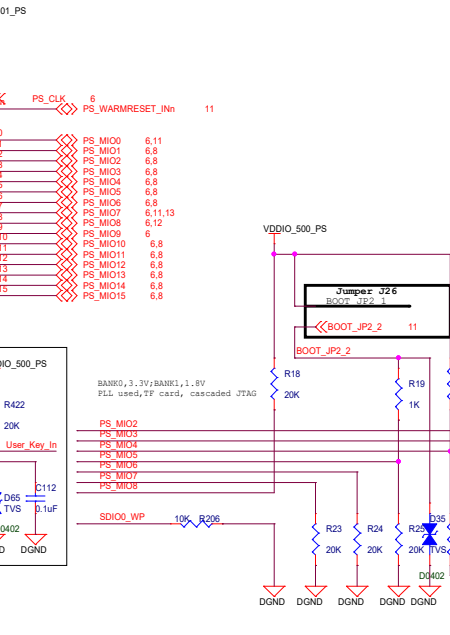
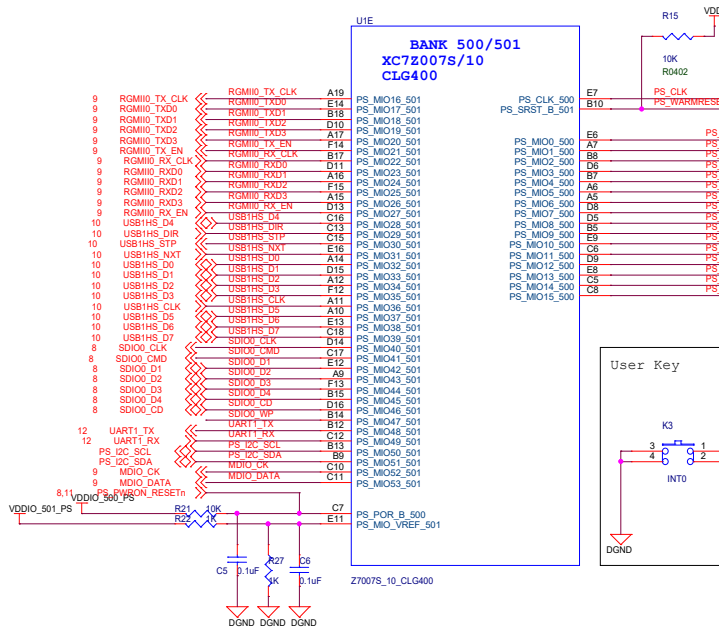
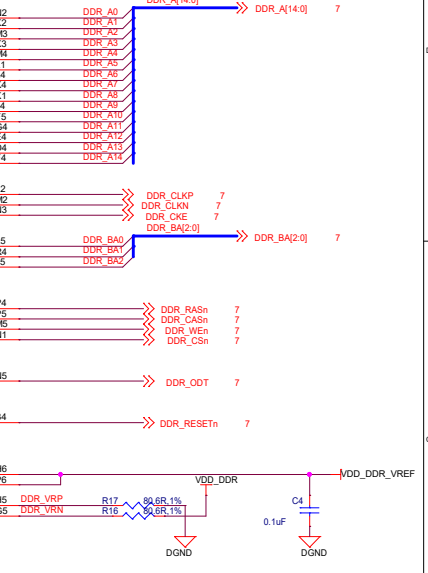
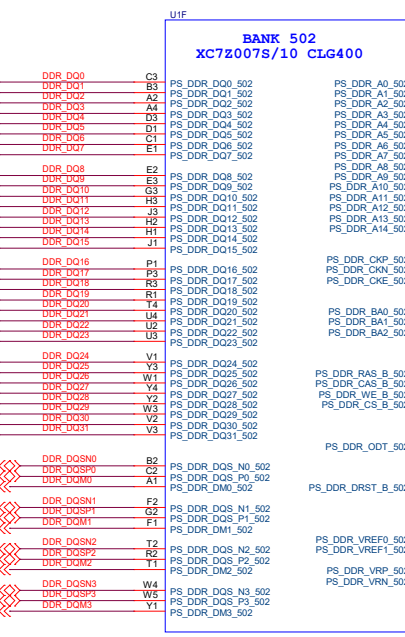
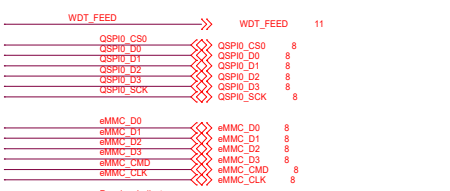
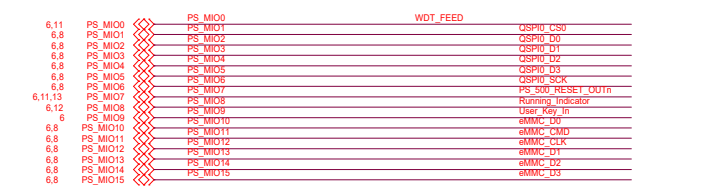
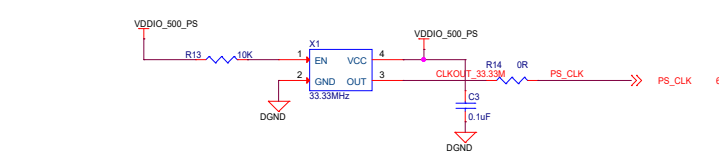
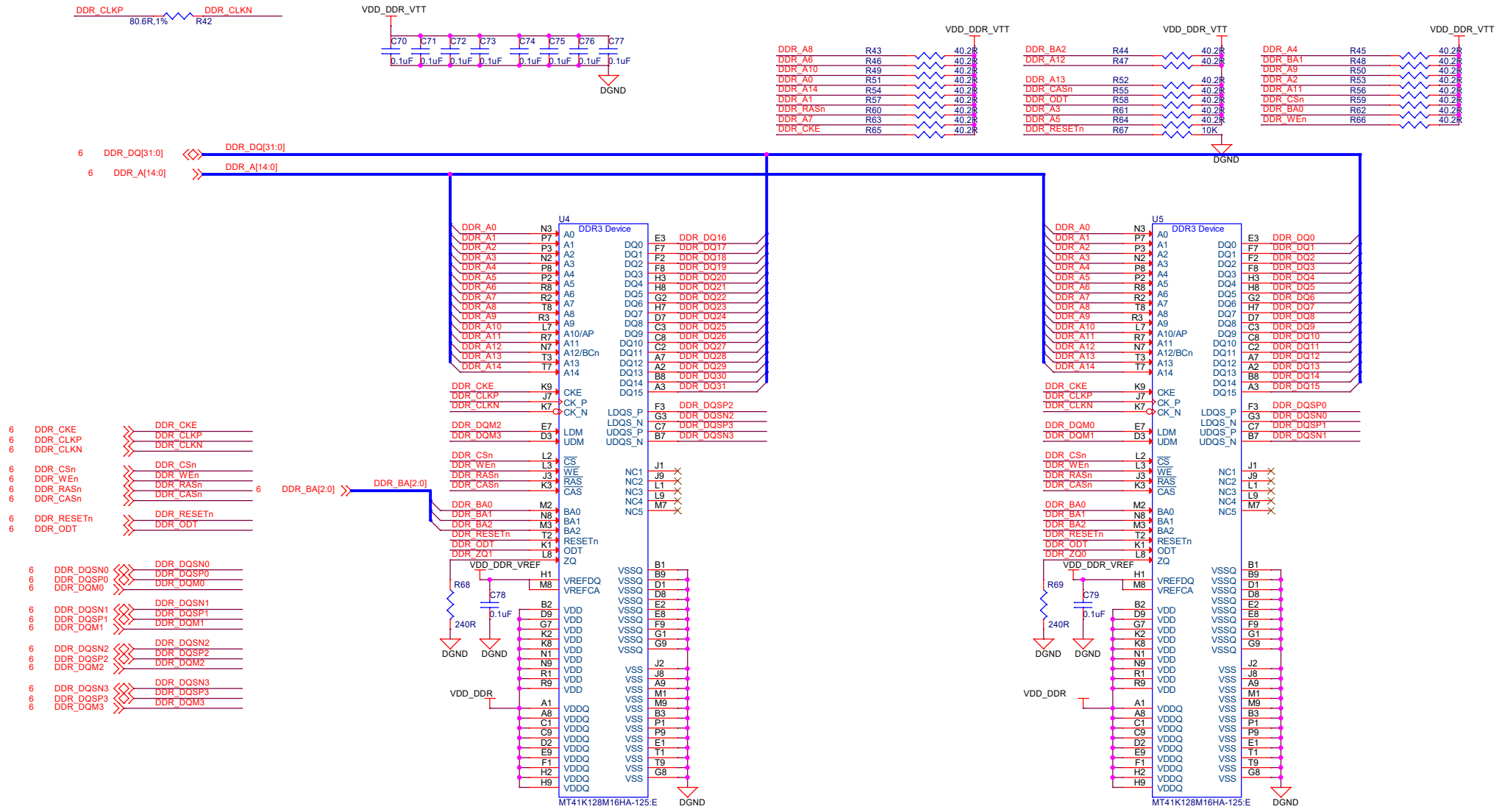


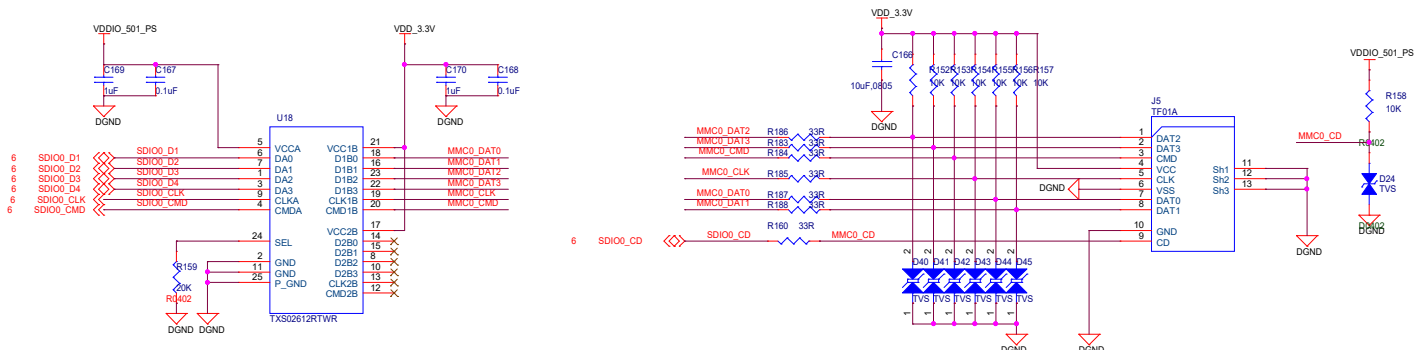
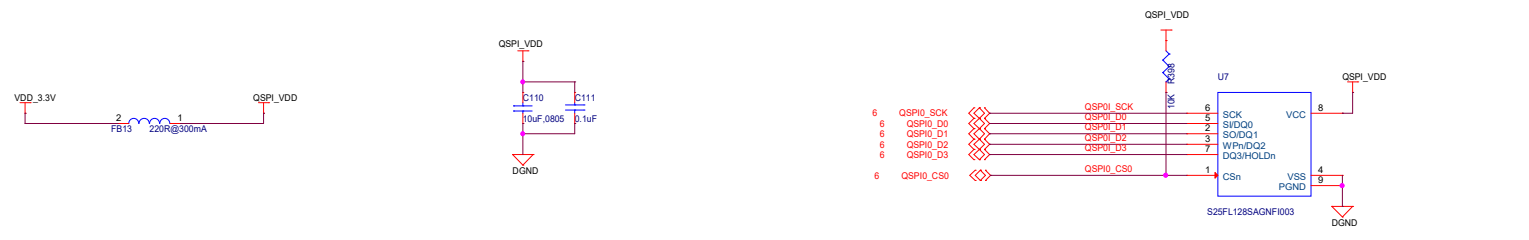
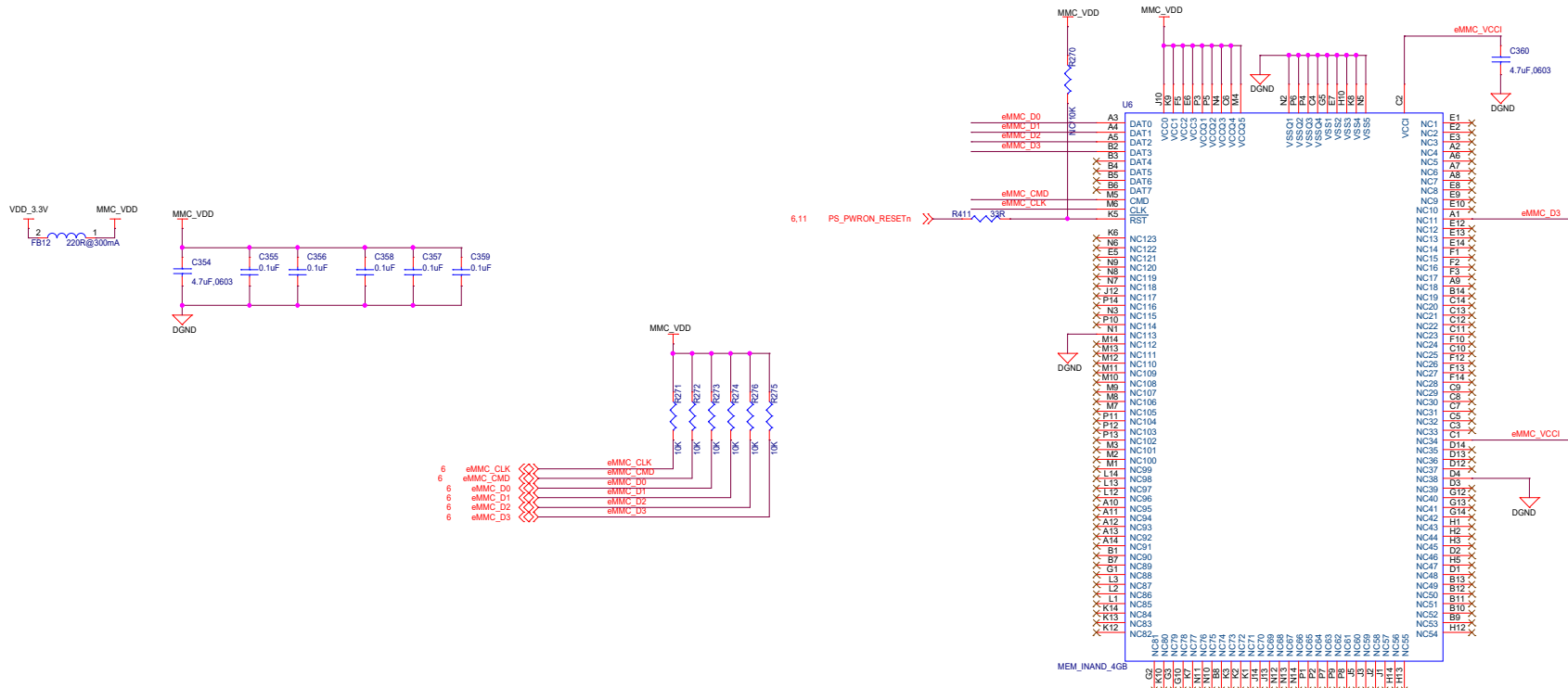
Table 6-2: Boot_Mode MIO Pins

| | VMODE[1] | VMODE[0] | BOOT_MODE [4] | BOOT_MODE [0] | BOOT_MODE [2] | BOOT_MODE [1] | BOOT_MODE [3] |
|--------------------|----------|----------|---------------|---------------|---------------|---------------|---------------|
| | MIO[8] | MIO[7] | MIO[6] | MIO[5] | MIO[4] | MIO[3] | MIO[2] |
| Cascaded JTAG | | | | | | | 0 |
| Independent JTAG | | | | | | | 1 |
| Boot Devices | | | | | | | |
| JTAG | | | 0 | 0 | 0 | 0 | 0 |
| NOR | | | 0 | 0 | 1 | 0 | |
| NAND | | | 0 | 1 | 0 | 0 | |
| Reserved | | | 0 | 1 | 1 | 1 | |
| Quad-SPI | | | 1 | 0 | 0 | 0 | |
| Reserved | | | 1 | 0 | 0 | 1 | |
| SD Card | | | 1 | 1 | 0 | 0 | |
| Reserved | | | 1 | 1 | 1 | 1 | |
| PLL Mode | | | | | | | |
| PLL Used | | | 0 | | | | |
| PLL Bypassed | | | 1 | | | | |
| MIO Bank 0 Voltage | | | | | | | |
| 2.5 V, 3.3 V | | | 0 | | | | |
| 1.8 V | | | 1 | | | | |
| MIO Bank 1 Voltage | | | | | | | |
| 2.5 V, 3.3 V | | | 0 | | | | |
| 1.8 V | | | 1 | | | | |

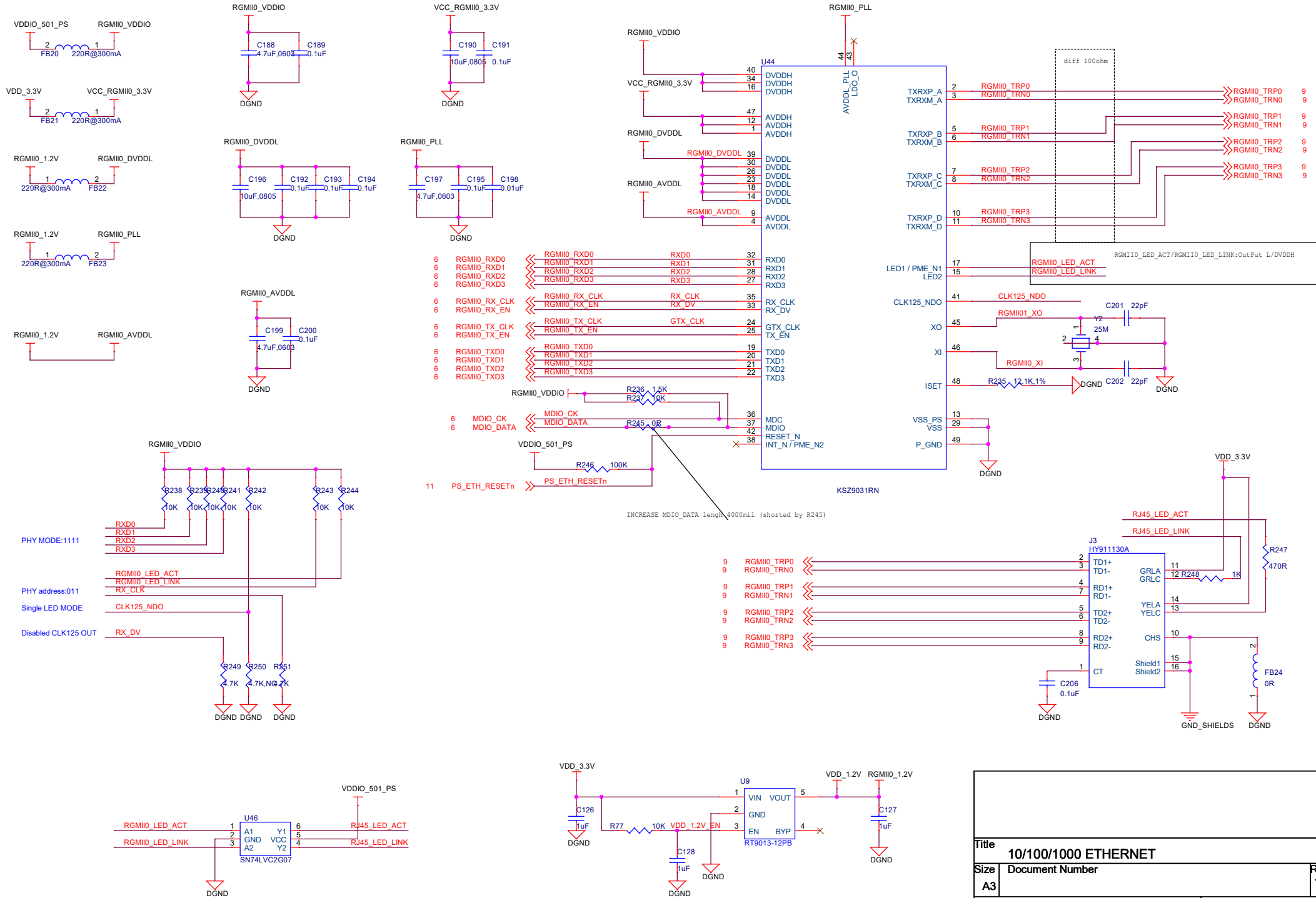
512MB DDR3 (x32)



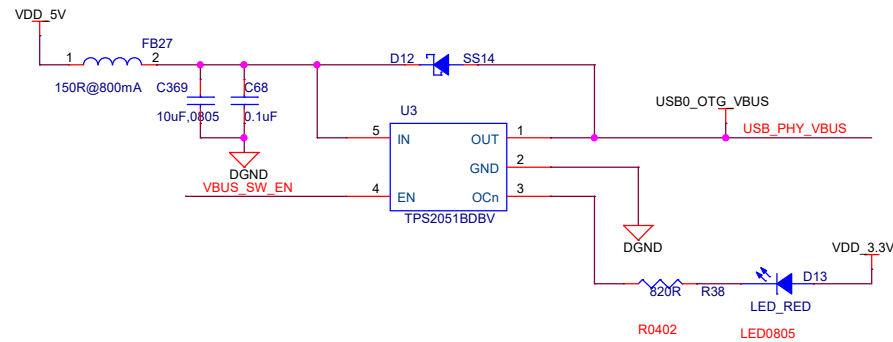
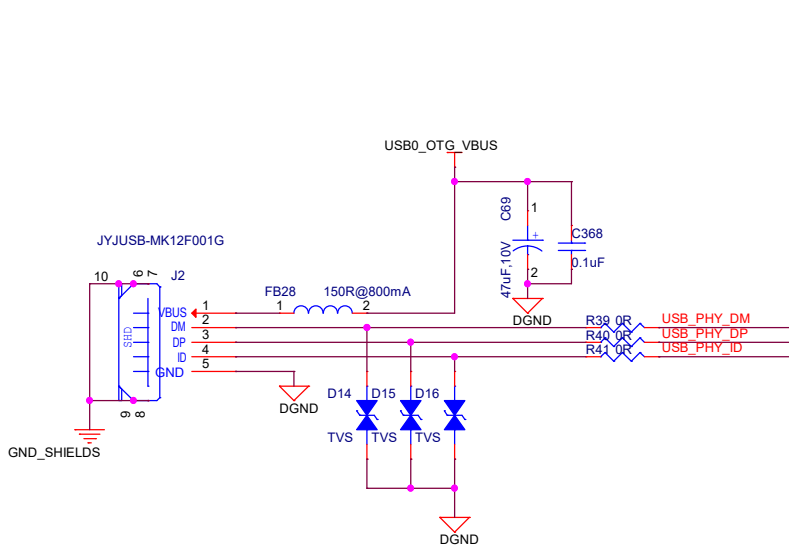
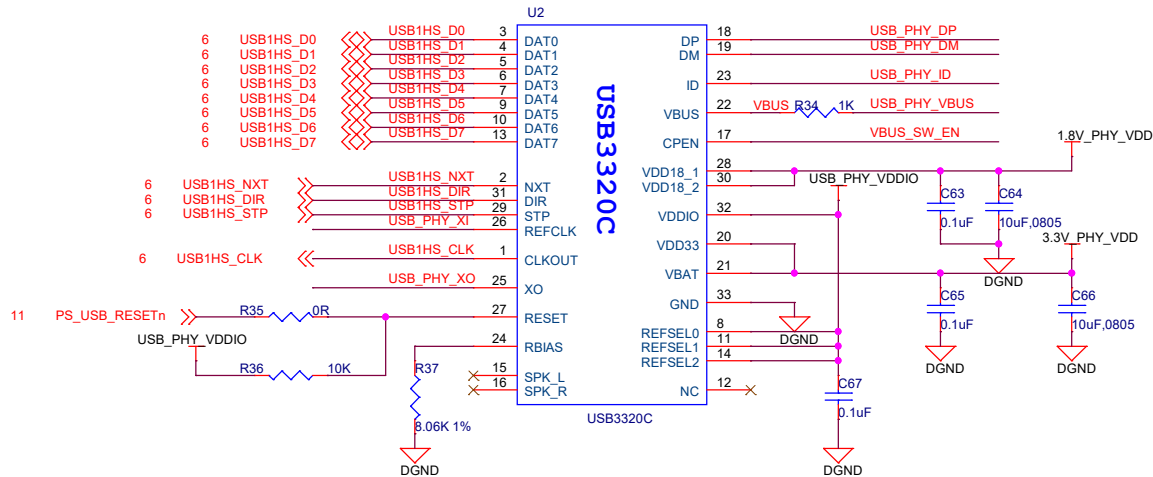
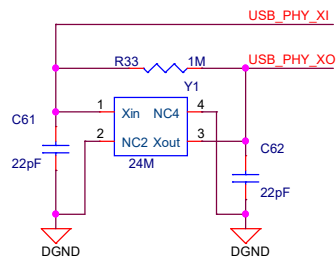
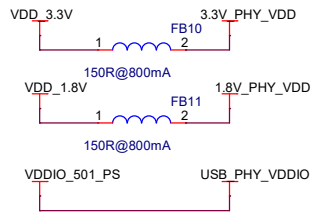
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|-------|------------------------|---------------|
| Title | | DDR3 MEMORY |
| Size | Document Number | |
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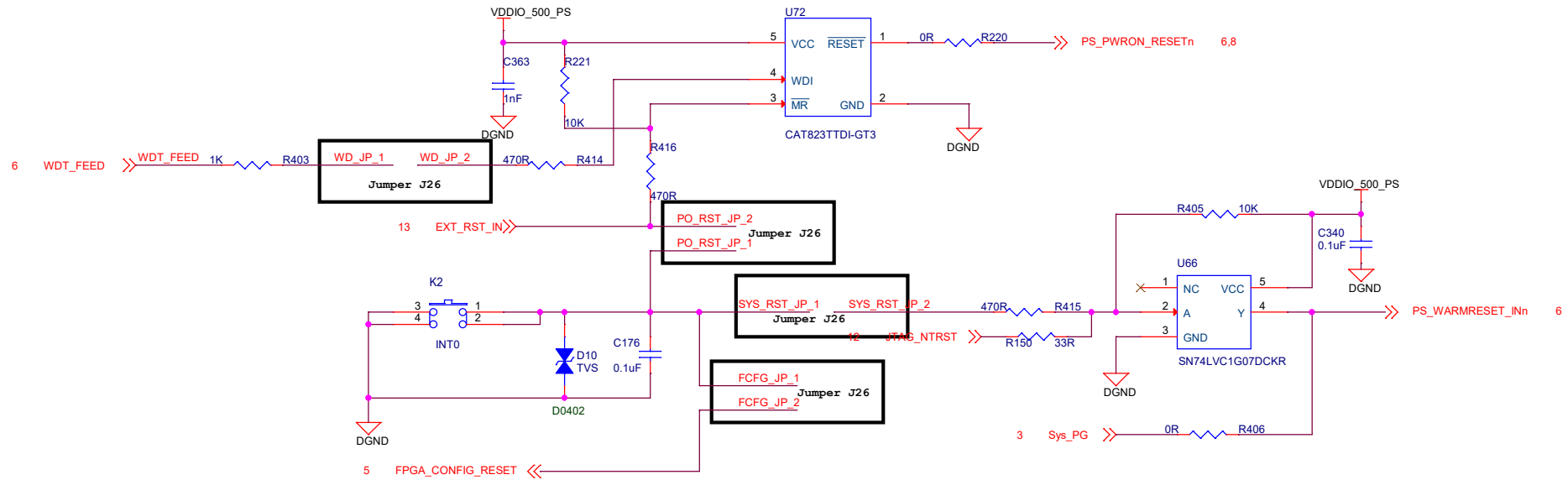
| | | |
|-------|------------------------|---------------|
| Title | QspiFlash & Emmc & TF | |
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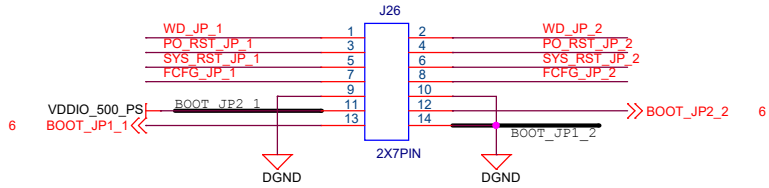
| | | |
|----------------------|------------------------|---------------|
| Title | | |
| 10/100/1000 ETHERNET | | |
| Size | Document Number | Rev |
| A3 | | V4.0 |
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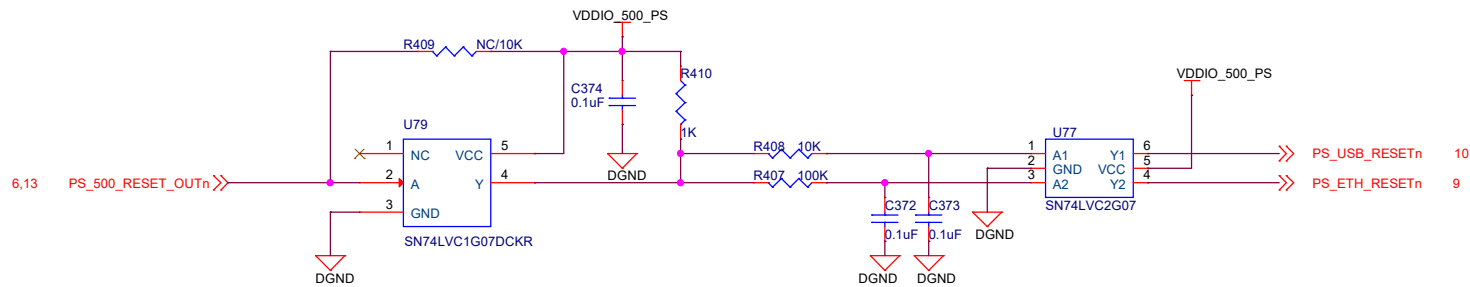
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| Title | | |
| USB OTG | | |
| Size | Document Number | Rev |
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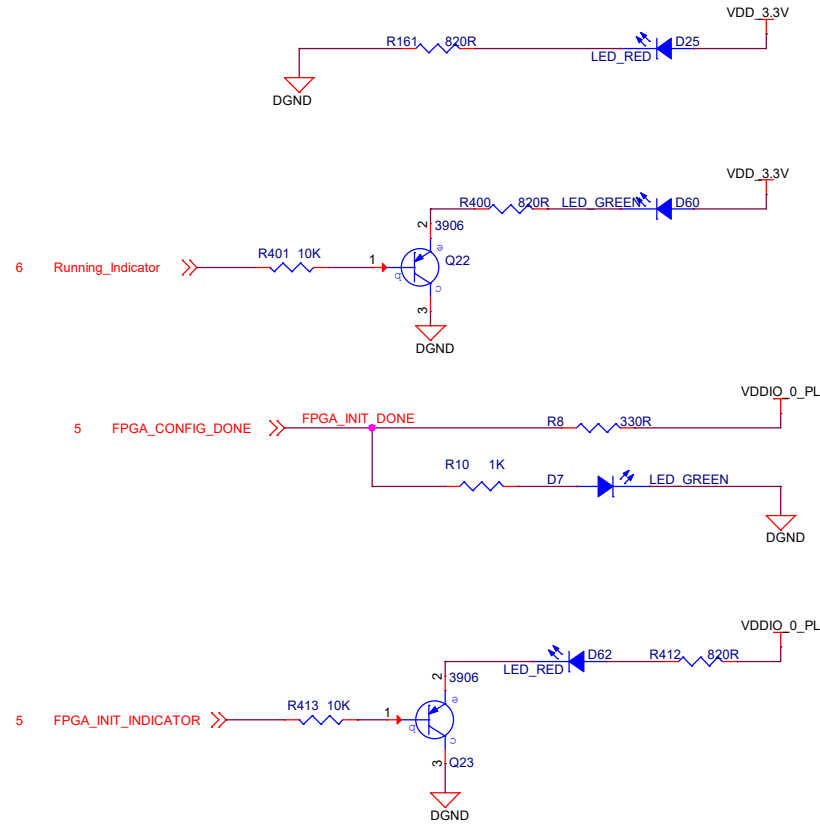
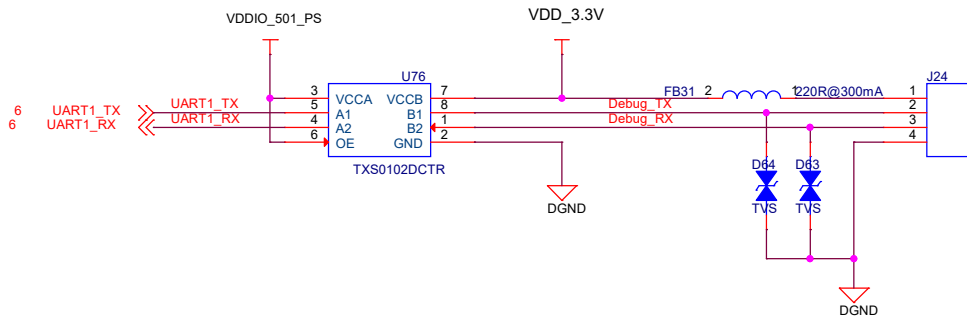
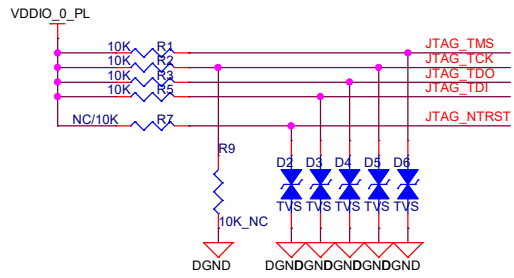
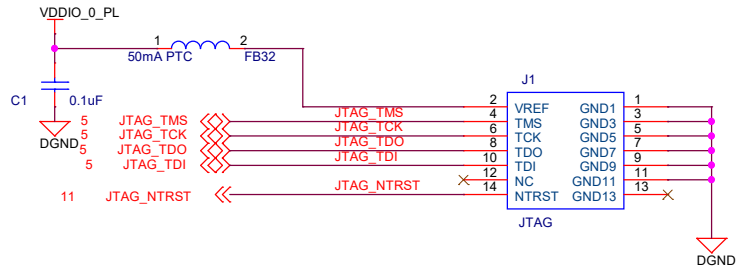
WD JP/PO RST JP/SYS RST JP/FCFG JP:
 WD_JP--Open to disable watchdog;
 --Close to enable watchdog.
 PO RST JP--Default open, closed when not in debug case.
 SYS RST JP--Default closed for system debug reset.
 FCFG JP--Default open, closed for FPGA PL debug.
 Only one jumper can be closed at the same time among PO_RST_JP/SYS_RST_JP/FCFG_JP.



BOOT JP1 & BOOT JP2:
 JP1/JP2 ON: QSPI(default)
 JP1 ON,JP2 OFF: JTAG
 JP1 OFF,JP2 ON:SD Card
 JP1 &JP2 OFF:NAND(undefined)

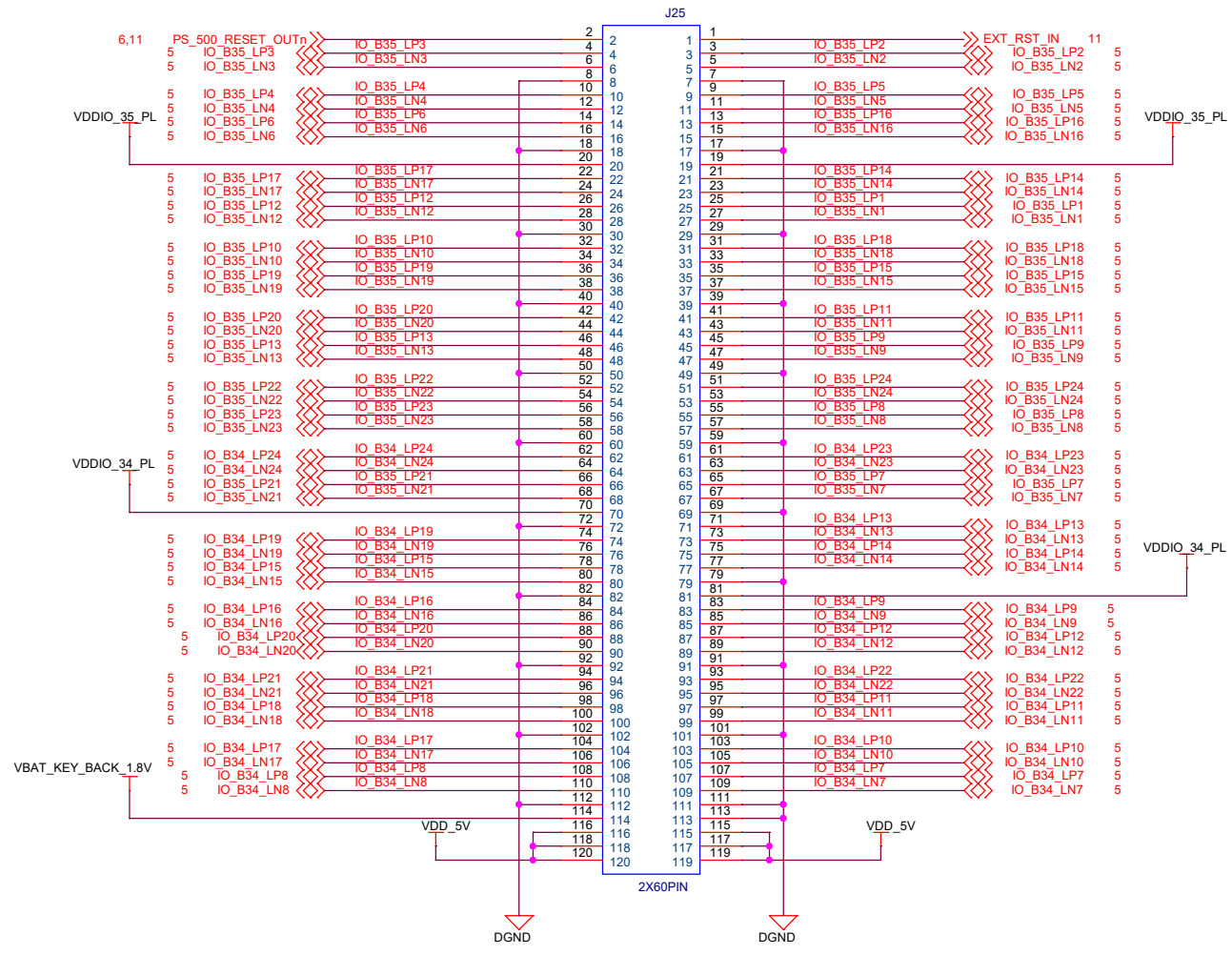


| | | |
|------------------|------------------------|----------------|
| Title | | |
| WatchDog & Reset | | |
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| | | |
|------------------------------|------------------------|----------------|
| Title | | |
| Jtag & DebugUart & StatusLed | | |
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Signals Out:
 BANK35 24 pairs of differential signals;
 BANK34 18 pairs of differential signals;
 PowerOnResetIn & SoftwareResetOut.



| | | |
|----------|------------------------|----------------|
| Title | | |
| Exp Conn | | |
| Size | Document Number | Rev |
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